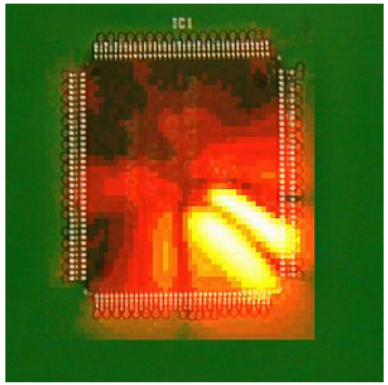
EMC of ICs Practical Trainings

IC-EMC

www.ic-emc.org



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Welcome to IC-EMC homepage

The IC-EMC software is a non-commercial tool dealing with electromagnetic compatibility (EMC) of integrated circuits (IC), and covering both parasitic emission and susceptibility to radio-frequency interference (more).

Based on 20 years of research, IC-EMC gathers a unique collection of IC models, tools and EMC measurements related to more than 15 IC case studies complied in a user's manual (more).

A user's manual describes the basic and advanced features of IC-EMC. Application notes described new case studies, specific tools and approaches (more). The tool is also used for trainings in university and in industry (more).

A five day training about EMC of ICs is proposed. Real case studies and pratical trainings are proposed based on IC-EMC. More information (here).

A book (more) is also proposed which basic notions for learning how to model circuits and their surrounding environment (PCB) with respect to emission, immunity and signal integrity issues. The book also provides a series of exercises. Corrections can be found here. (more)

WinSpice

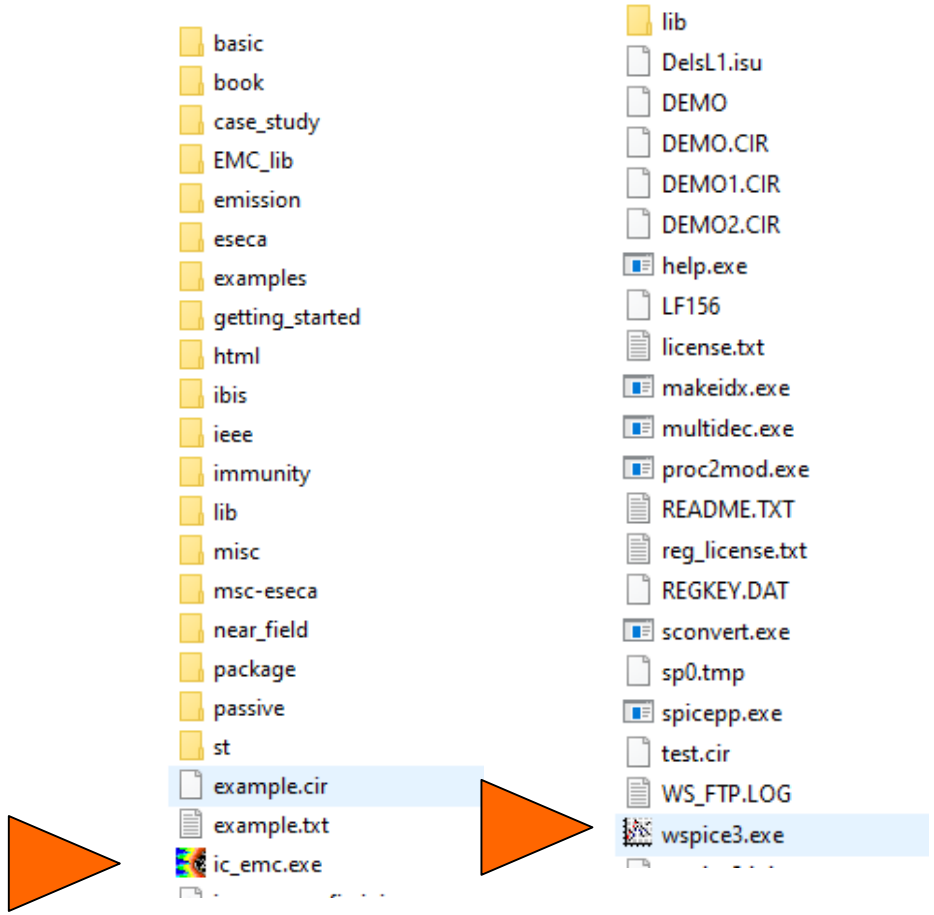
http://www.winspice.com/

Unzip

- Unzip both files in \documents

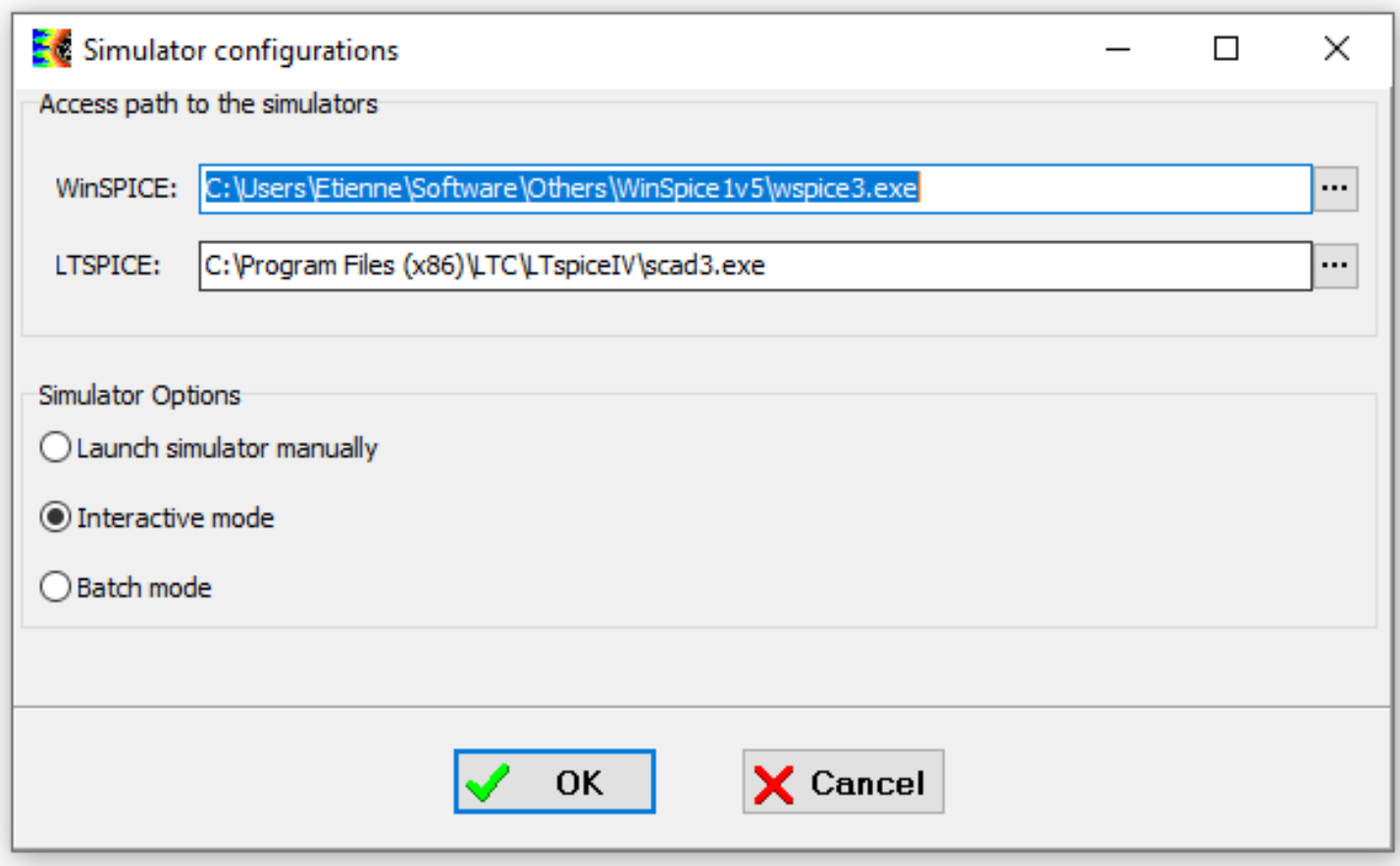
IC-EMC-2v9.zip

WinSpice1v5.zip



Configure IC-EMC

- Find wspice.exe



Objectives

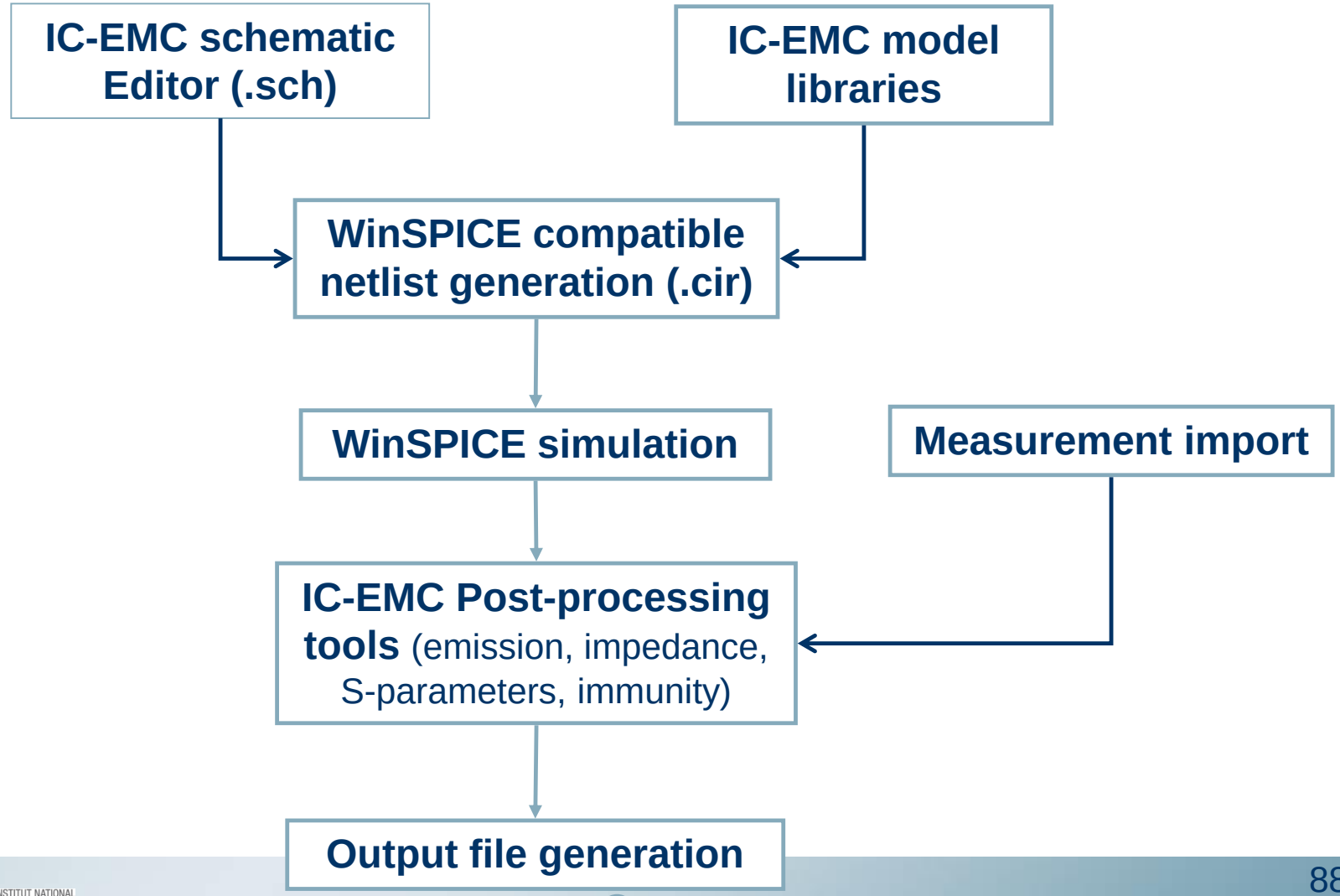
- Get familiar with IC-EMC/Winspice
- Illustrate parasitic emission mechanisms
- Understand parasitic emission reduction strategies
- Power Decoupling Network modelling
- Basis of conducted and radiated emission modelling
- Basis of immunity modelling

Summary

- IC-EMC – Reference
- Ex. 1. FFT of typical signals
- Ex. 2. Transient current estimation
- Ex. 3. Interconnect parasitics
- Ex. 4. Impedance mismatch
- Ex. 5. di/dt noise
- Ex. 6. intrinsic decoupling
- Ex. 7. added on-chip decoupling
- Ex. 8. PDN modelling
- Ex. 9. Radiated emission modelling

- Ex. 10. Estimation of susceptibility level
- Ex. 11. Susceptibility of analog input
- Ex. 12. Susceptibility of output buffer
- Ex. 13. Susceptibility of a micro-controller

IC-EMC - Simulation flow

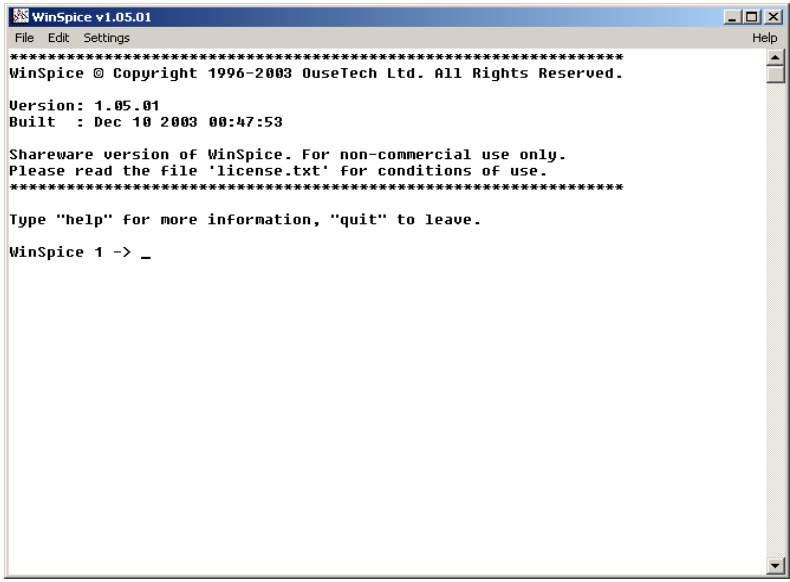


IC-EMC – Most Important Icons

	Open schematic (.sch)		Build SPICE netlist (.cir)
	Save schematic (.sch)		Spectrum analysis
	Delete symbols		Near field emission simu.
	Copy symbols		Immunity simulation
	Move symbols		Time domain analysis
	Rotate symbols		Impedance simulation
	Flip symbols		S parameter simulation
	Add Text line		Ibis file editor
	Add a line		Parametric analysis
	View electrical net		Symbol palette
	Zoom in/out		View all schematic

IC-EMC – Link to WinSpice

- Click on WinSPICE.exe
- Click File/Open to open a circuit netlist (.cir) generated by ic-emc.

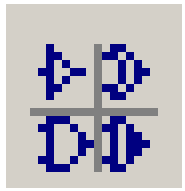


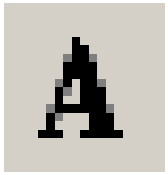
- IC-EMC main commands (text line):

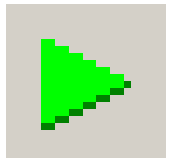
Simulation command	Command line	Parameters
Transient simulation	**.tran 0.1n 100n**	**step + stop time**
DC simulation	**.DC Vdd 0 5 0.1**	**source + start + stop + step**
Small signal freq. analysis	**.AC DEC 100 1MEG 1G**	**sampling + nb points + start + stop**
Load SPICE library	**.lib 65nm.lib**	**Path and file name**

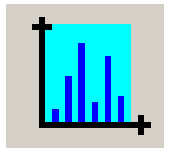
Exercise 1. FFT of typical signals

- Create the schematic
- Set the source generator
- Transient simulation
- FFT by IC-EMC
- Simulate the FFT of a sinus and a square signal



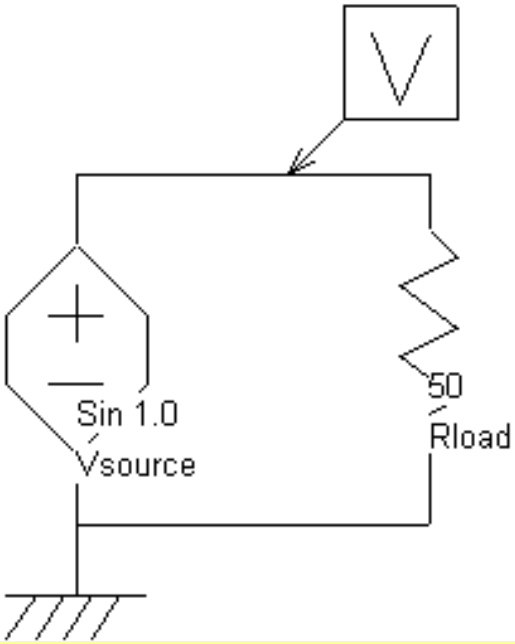




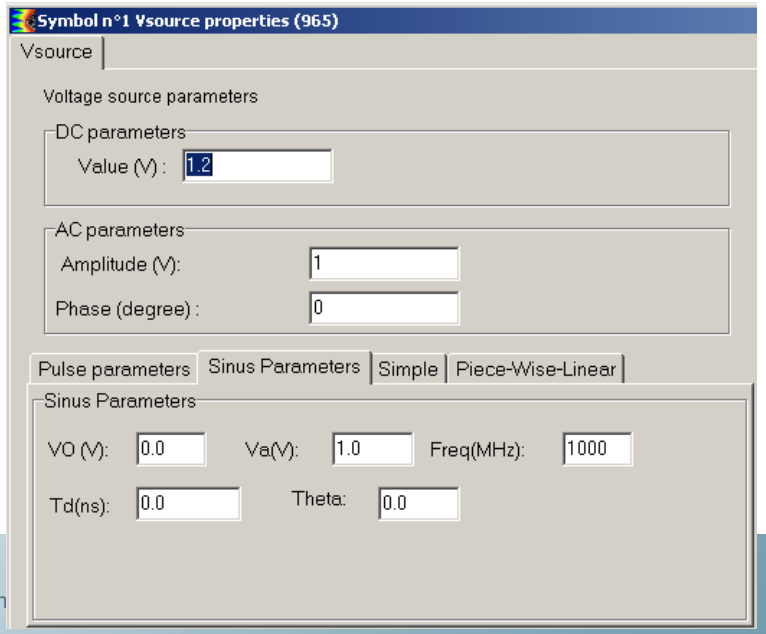


Exercise 1. FFT of typical signals

- FFT of a sinus source
  - Set the voltage generator properties:
    - Frequency = 1 GHz
    - Amplitude = 1 V

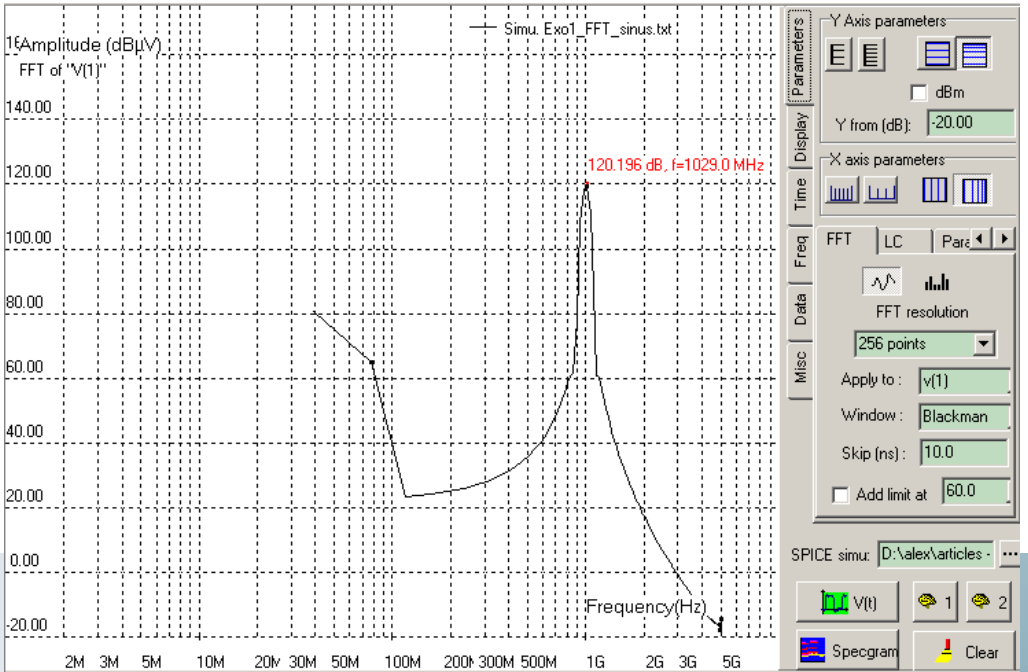


Ex1-FFT-sinus.sch



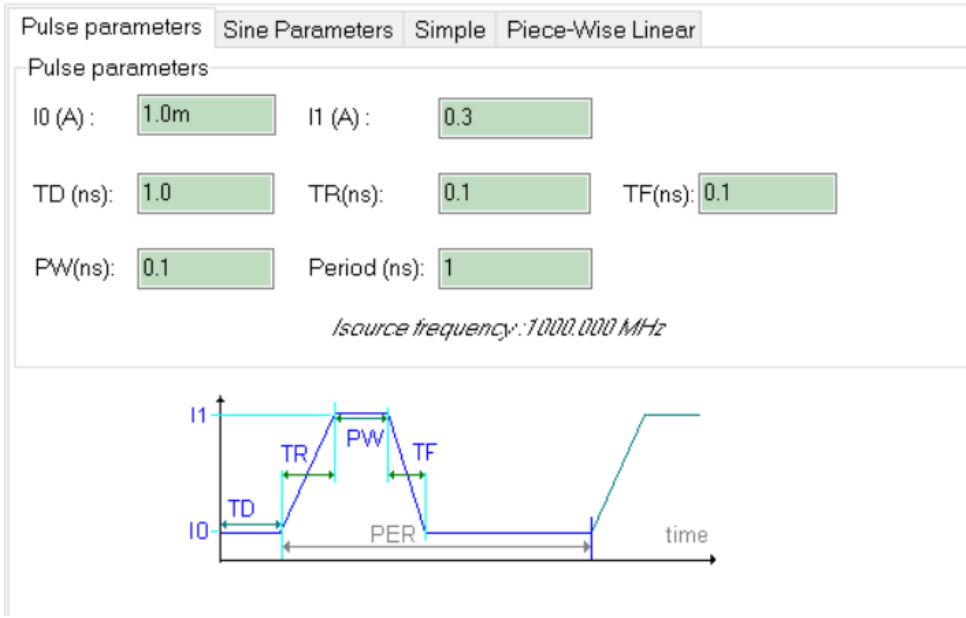
Exercise 1. FFT of typical signals

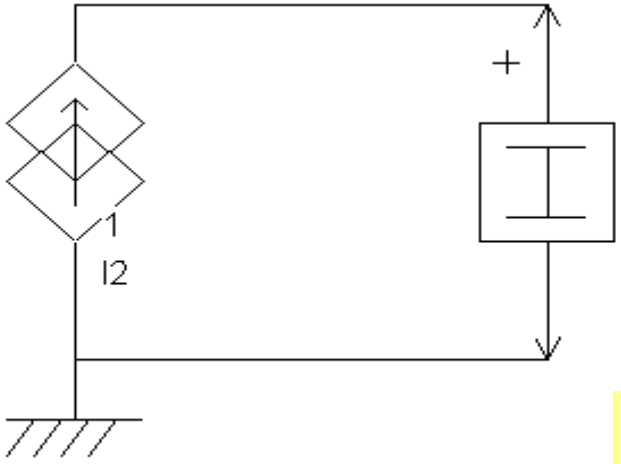
- FFT of a sinus source
  - Type the simulation command: .tran 1n 50n
  - Simulate the response in time domain.
  - Compute the FFT.
  - Does the FFT result correlate with theoretical result ?



Exercise 1. FFT of typical signals

- FFT of a square current source
  - Set the generator properties
  - For example:
    - Period = 1 n,
    - PW as small as possible
    - Tr = 0.1n, Tf = 0.1 n
    - V0 = 0 V, V1 = 0.9 V





Ex1-FFT-Pulse.sch

Exercise 1. FFT of typical signals

- FFT of a square source

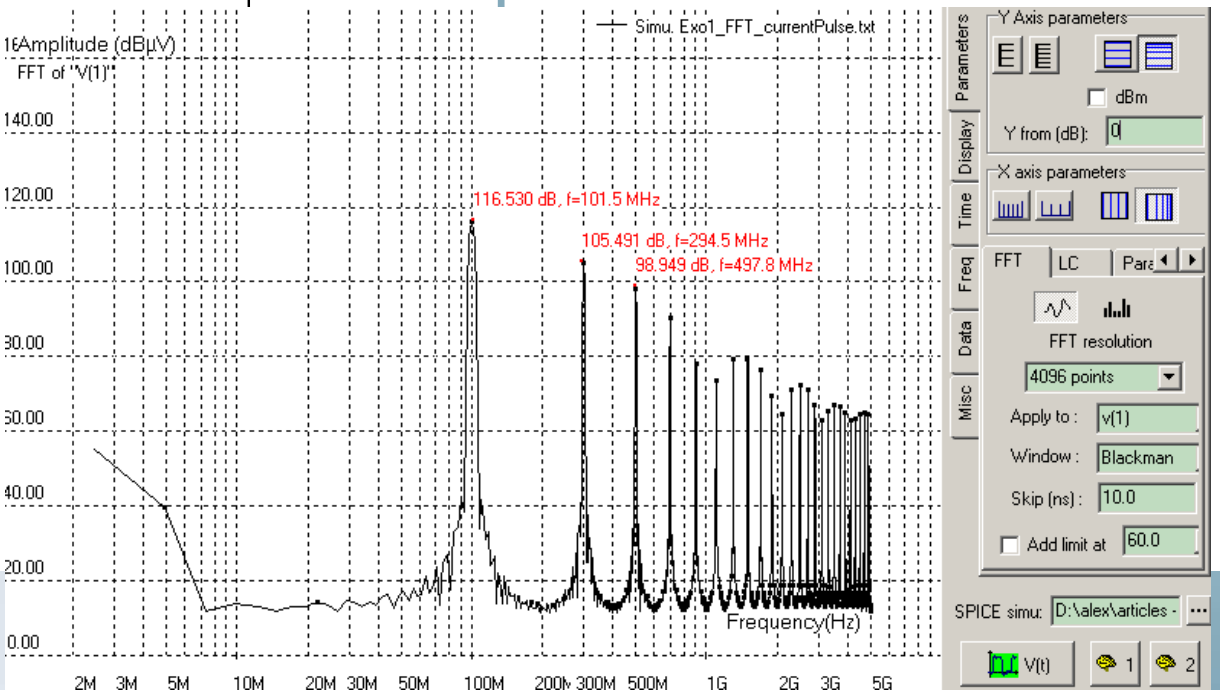
For a square signal (Tr=0)

$$\left|c_n^+\right| = \frac{2A\tau}{T}\left|\frac{\sin\left(n\pi\frac{\tau}{T}\right)}{n\pi\frac{\tau}{T}}\right|, n>0$$

$$c_0 = \frac{A\tau}{T}$$

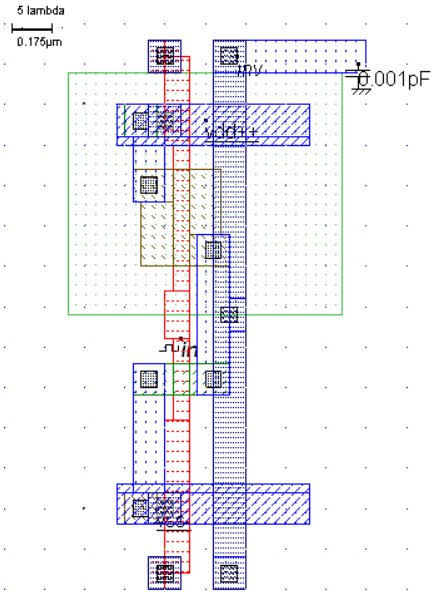
For a trapezoidal signal (Tr=Tf)

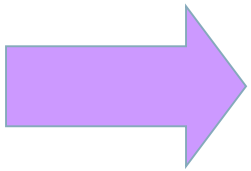
$$\left|c_n^+\right| = \frac{2A\tau}{T}\left|\frac{\sin\left(n\pi\frac{\tau}{T}\right)}{n\pi\frac{\tau}{T}}\right|\left|\frac{\sin\left(n\pi\frac{t_r}{T}\right)}{n\pi\frac{t_r}{T}}\right|, n>0$$

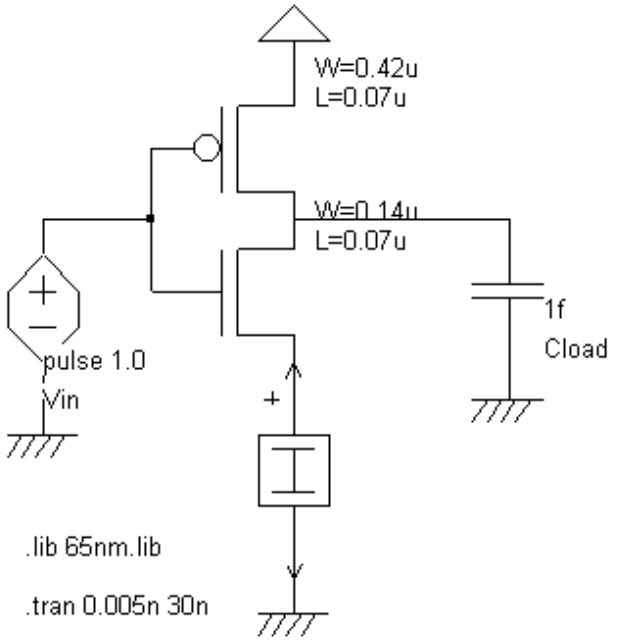


Exercise 2. Transient current estimation

- Standard cell inverter in CMOS technology
- Typical load capacitance
- Observe in time domain the current through Vss.



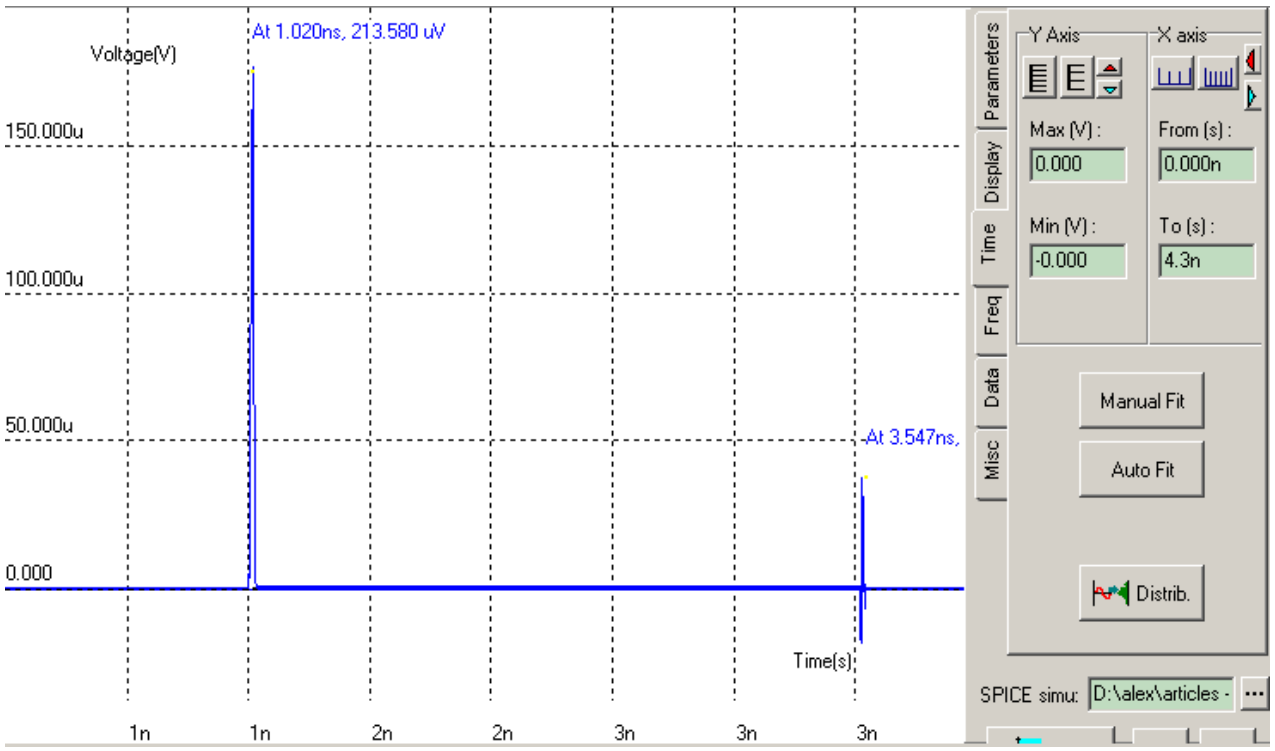




Ex2-transient_inverter.sch

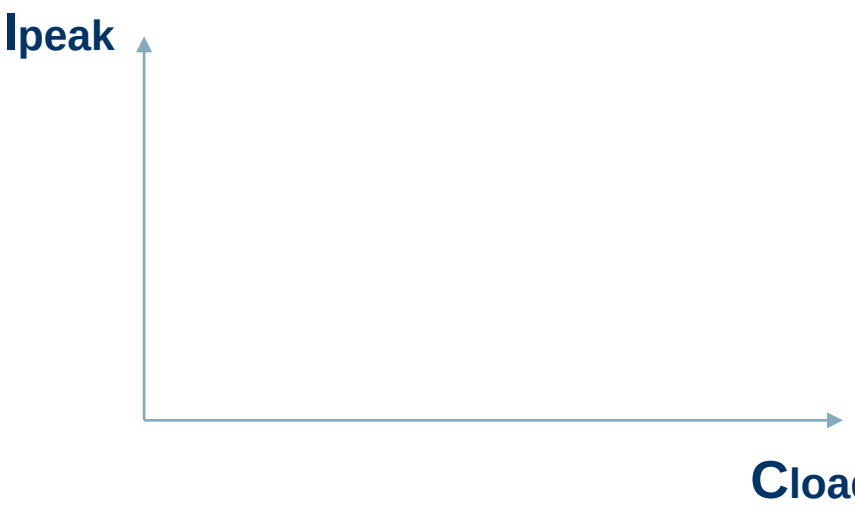
Exercise 2. Transient current estimation

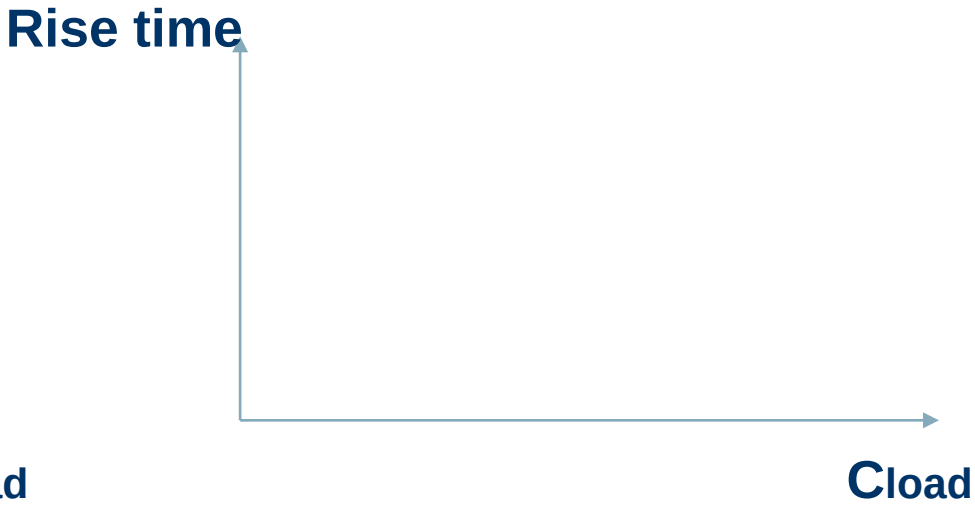
- Time domain simulation
- Adjust scales (Autofit and zoom on time axis)



Exercise 2. Transient current estimation

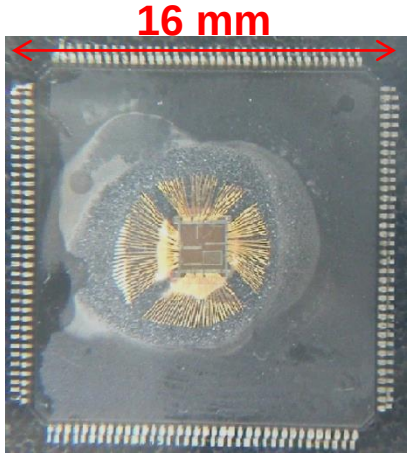
- What is the influence of the load capacitance (1 fF to 1 pF) ?

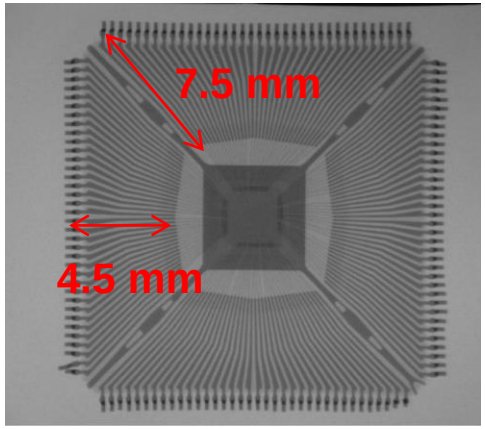


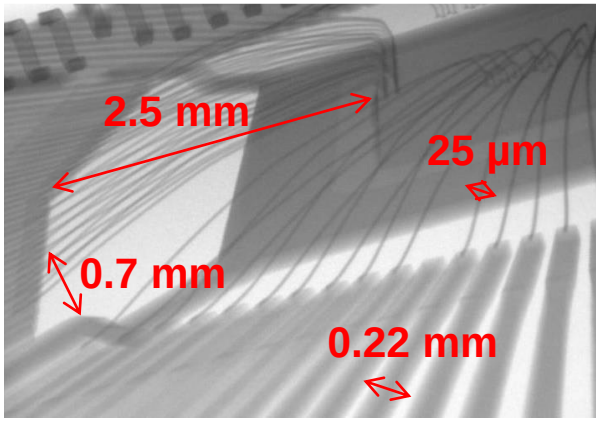


Exercise 3. Interconnect parasitics

- The core is mounted in a QFP100 package.
- A pair of pins is dedicated to supply the core







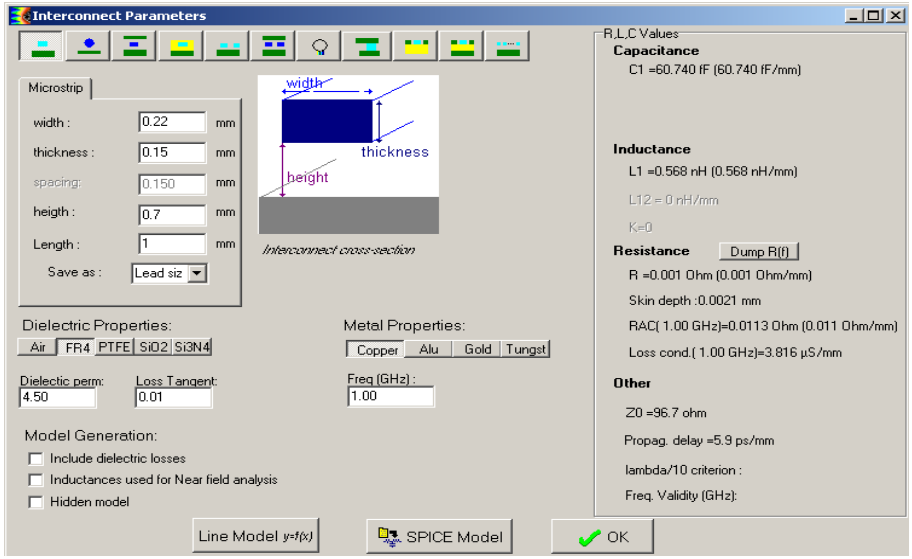
Evaluate the electrical parasitic associated to the power supply pair.

Exercise 3. Interconnect parasitics

Use Tools/Interconnects Parameters to evaluate R, L, C associated to package pins.

Empirical estimation :

- Lead : L = 0.5 nH/mm and C = 0.1 pF/mm
- Bonding : L = 1 nH/mm

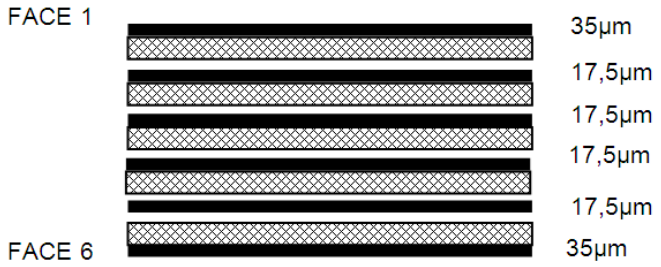


$$L = \frac{\mu_o l}{2\pi} \ln\left(\frac{8h}{W} + \frac{W}{4h}\right)$$

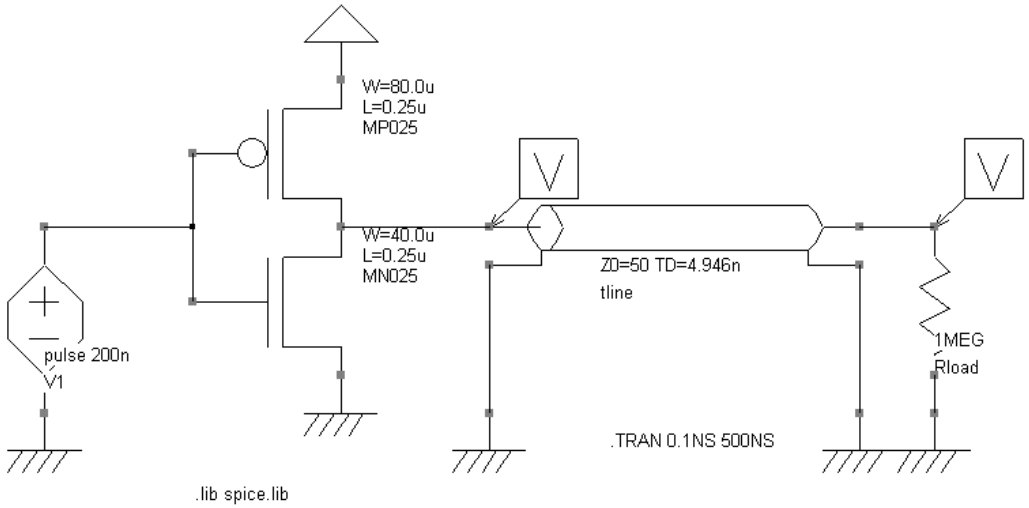
$$L = \frac{\mu_o l}{2\pi} \times \ln\left(\frac{4h}{r}\right)$$

Exercise 4. Impedance Mismatch

- Generate a fast clock
- Load a transmission line model
- Terminate by a high impedance
- Terminate by 50 Ω

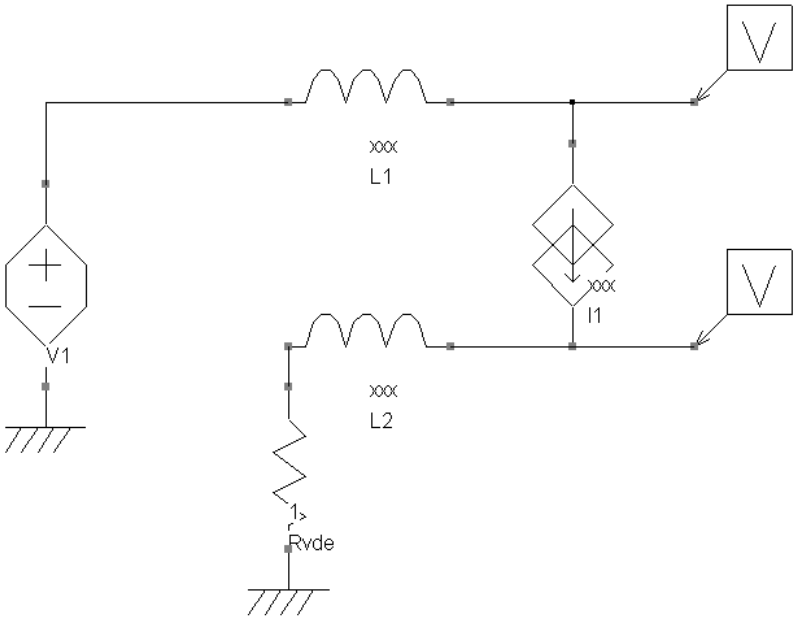


1.6mm total



Exercise 5. di/dt noise

- Estimate the voltage bounce on Vdd and Vss pins of the core when it is mounted in a QFP 64.
- The core clock is 20 MHz.

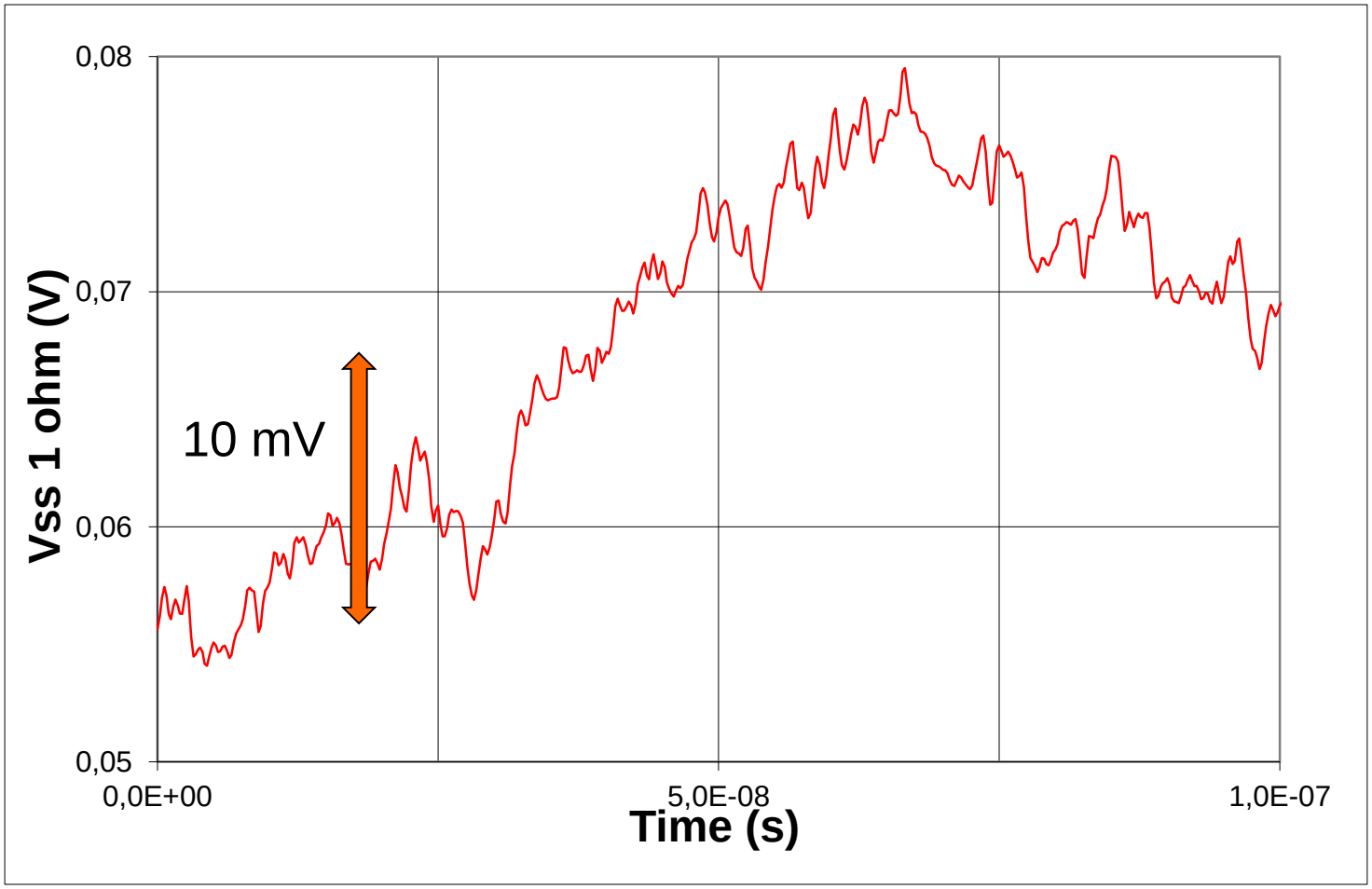


$$\Delta V = ?$$

Core noise margin ?

Ex4-didt_noise.sch

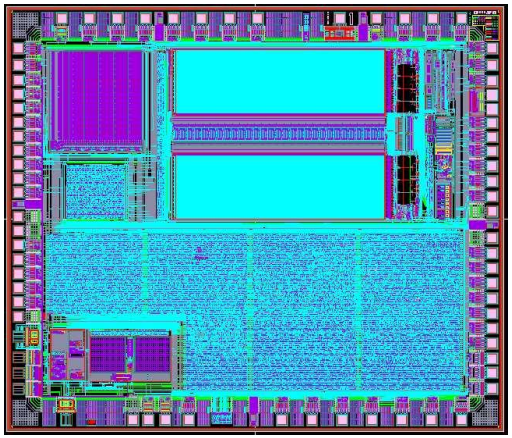
Exercise 5. di/dt noise



Exercise 6. Intrinsic decoupling

IC-EMC reference manual p. 18

Consider a synchronous digital core in CMOS 65 nm formed by 100 000 gates with the following parameters



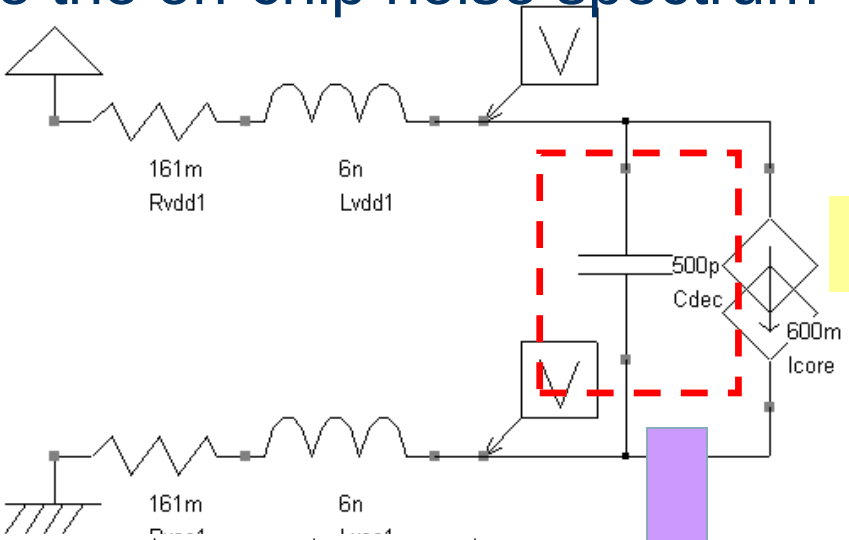
Std cell	Number	Typical input capa (fF)	Peak current / gate (µA)
Inverter	35000	1	120
NAND2	25000	1	150
DREG	20000	2	200
NOR2	20000	1	150

Estimate the intrinsic decoupling

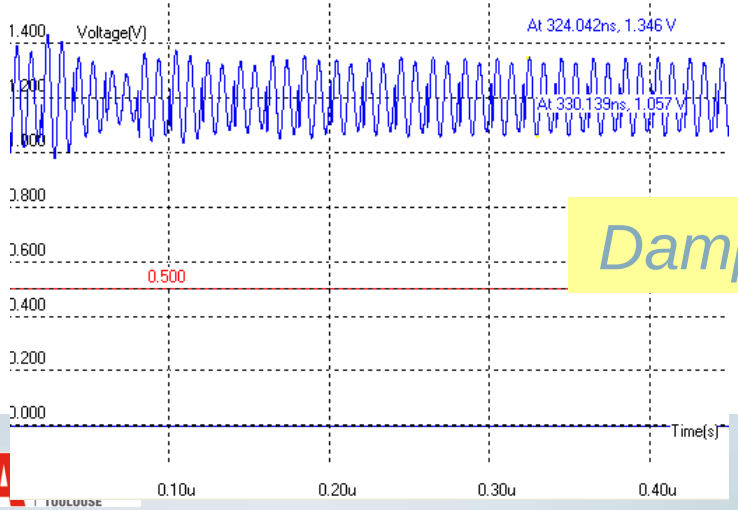
Estimate the dynamic current consumed by the circuit.

Exercise 6. Intrinsic decoupling

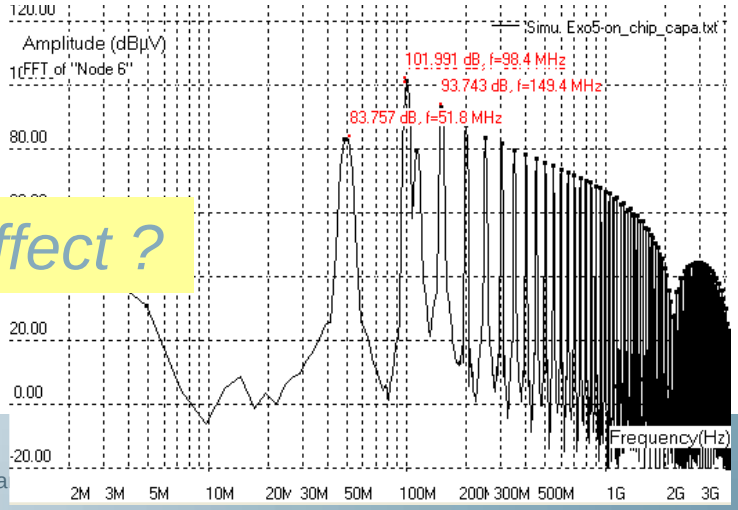
Compute the on-chip noise spectrum



Ex5-IntrinsicDecoupling.sch



Damping effect ?



Exercise 7. Added on-chip decoupling

IC power supply rails parasitics

- Consider a 1 mm long and 40 µm wide Vdd or Vss line.

Metal level	Thickness	Height to substrate
M6	0.4 µm	4.5 µm
M5	0.4 µm	3.3 µm
M1	0.3 µm	0.5 µm

- Total Inductance and resistance of chip power supply rails ?

Exercise 7. Added on-chip decoupling

On-chip capacitor budget :

$$\Delta i = C\frac{\Delta v}{\Delta t} \Leftrightarrow C = \frac{\Delta i \times \Delta t}{\Delta v}$$

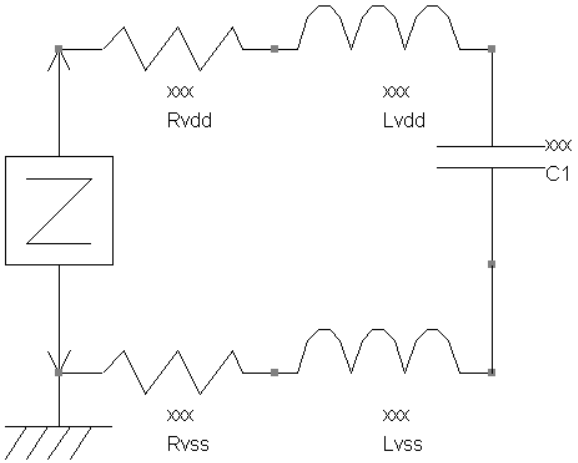
- Is the intrinsic capacitance is sufficient to reach the noise margin target ?
- How much capacitance should be added in the circuit ?

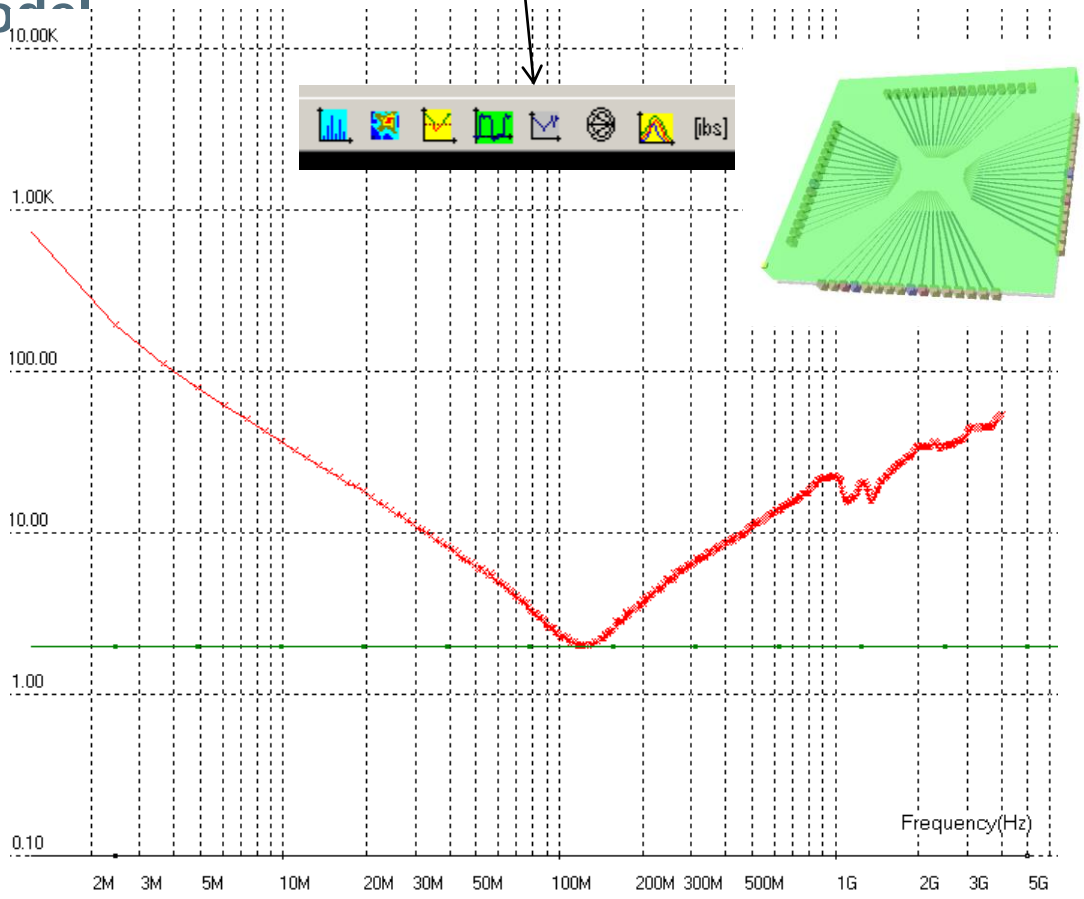
Capa. type	Capacitor density (fF/µm²)
Capa cell	2.2
Poly1 – Poly2	1.7
MIM	1.4

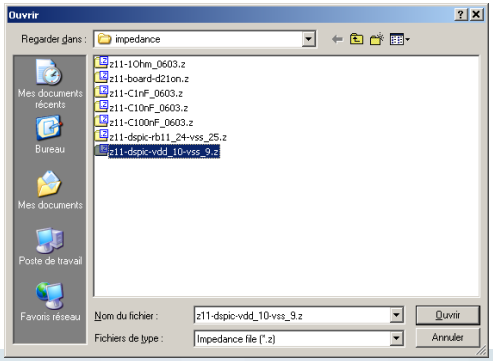
Ex6-AddRonChipC.sch

Exercise 8. PDN Modelling

- DSPIC Z(f): find an R,L,C mod
- Tune to measurement file:



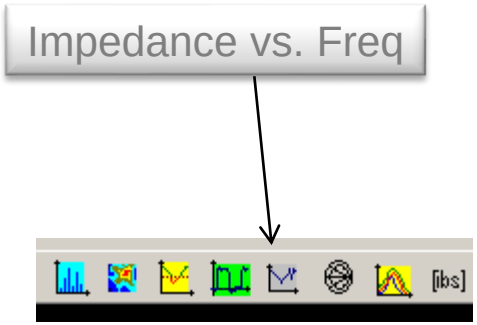


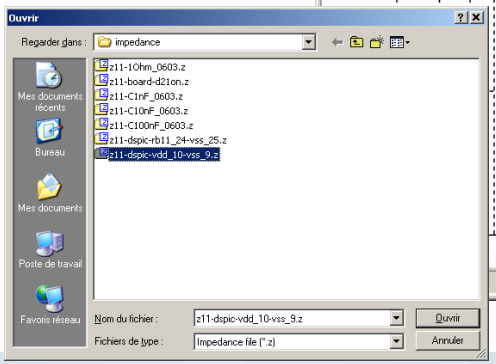


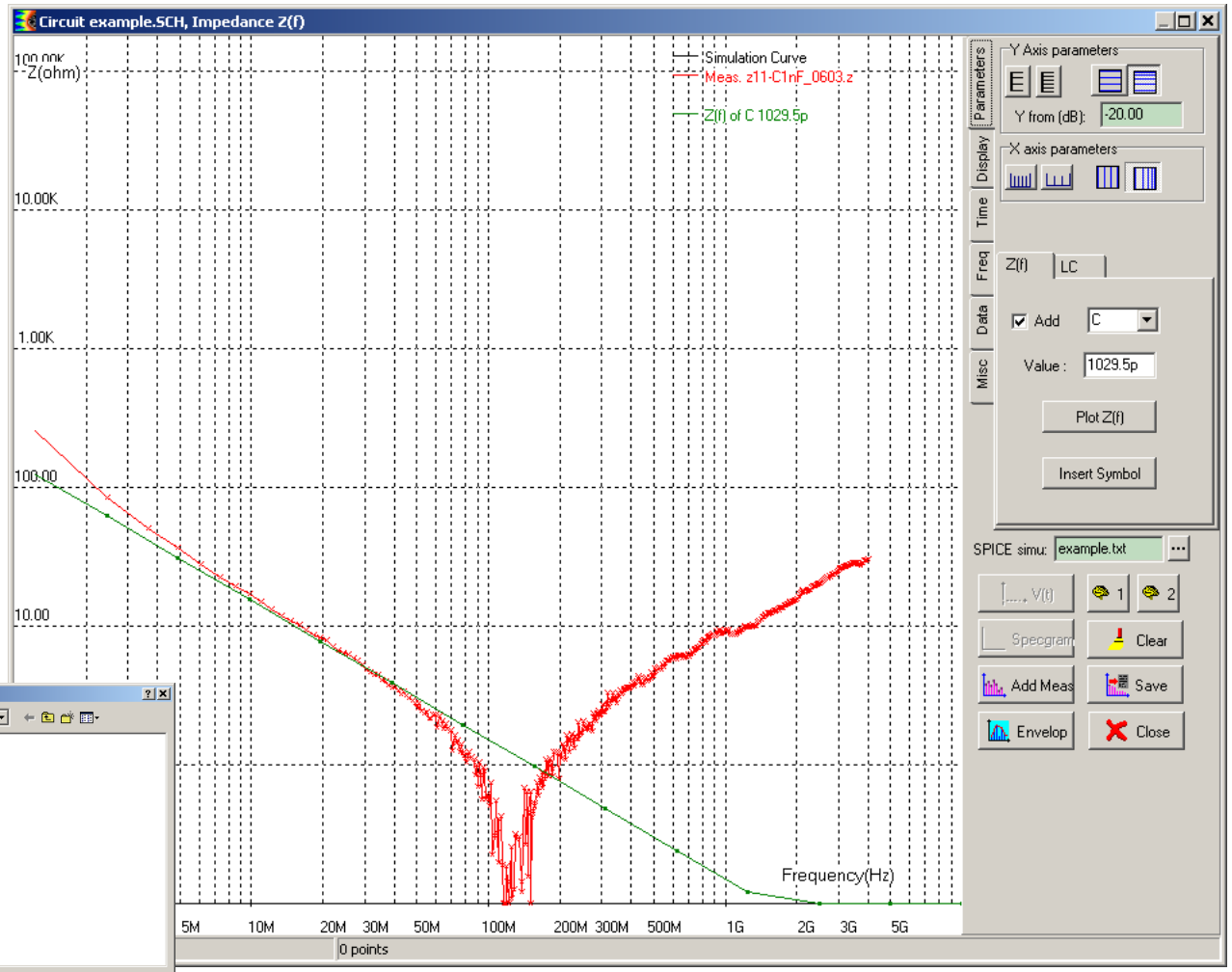
z11-dspic-vdd_10-vss_9.z

Exercise 8. PDN Modelling

- **z11-C1nF_0603.z**
- 1nF discrete capacitance for DPI





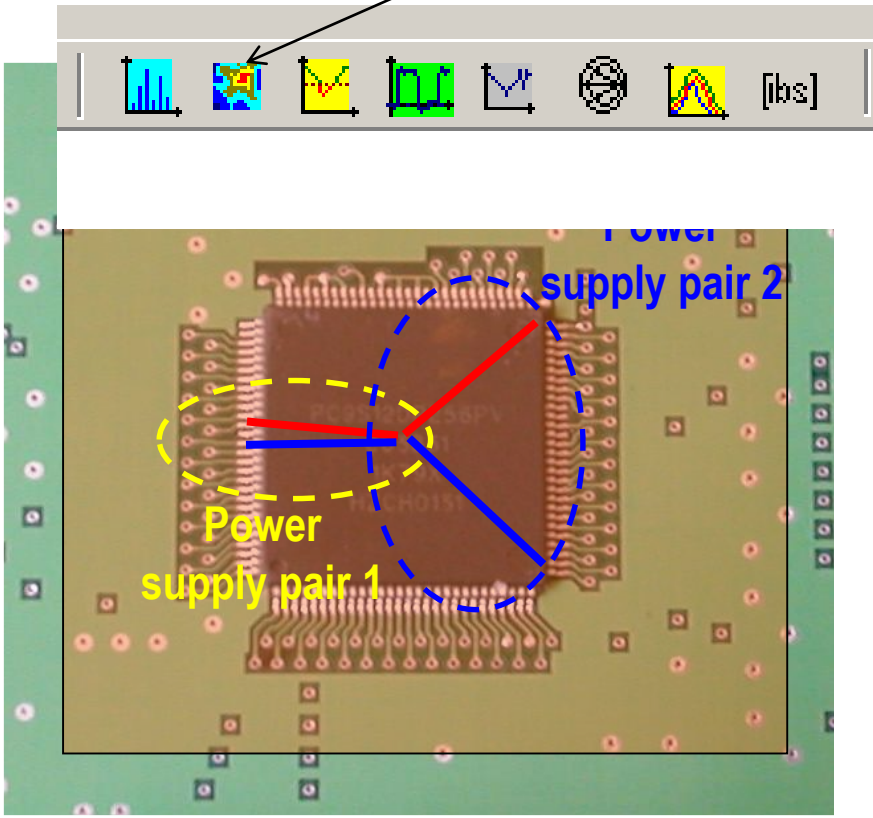


Exercise 9. Radiated Emission Modeling

- The circuit studied in exercise 5 is mounted in a QFP package.
- Two mounting versions, depending on the power supply pair assignment (pair 1 or pair 2)
- Its magnetic field emission is characterized by near field scan at 100 MHz.

- Compute the magnetic field at 1 mm above the package for both configurations.
- Conclude about the effect of power supply pair placement.

Ex8-RadEmi_Config1.sch and Ex8-RadEmi_Config2.sch



- Package geometry:
  - Width and height = 16 mm
  - Package pitch = 0.5 mm
  - Lead frame height = 0.7 mm

Exercise 9. Radiated Emission Modeling

- Compute the magnetic field at 1 meter above the package for both configurations.
- The following table gives the limit for radiated emission at 1 meter from electronic equipment, defined by CISPR 25.
- Does the circuit complies with CISPR 25 radiated limit at 100 MHz ?

CISPR 25 – Limits for narrowband radiated emission at 1 m from equipment

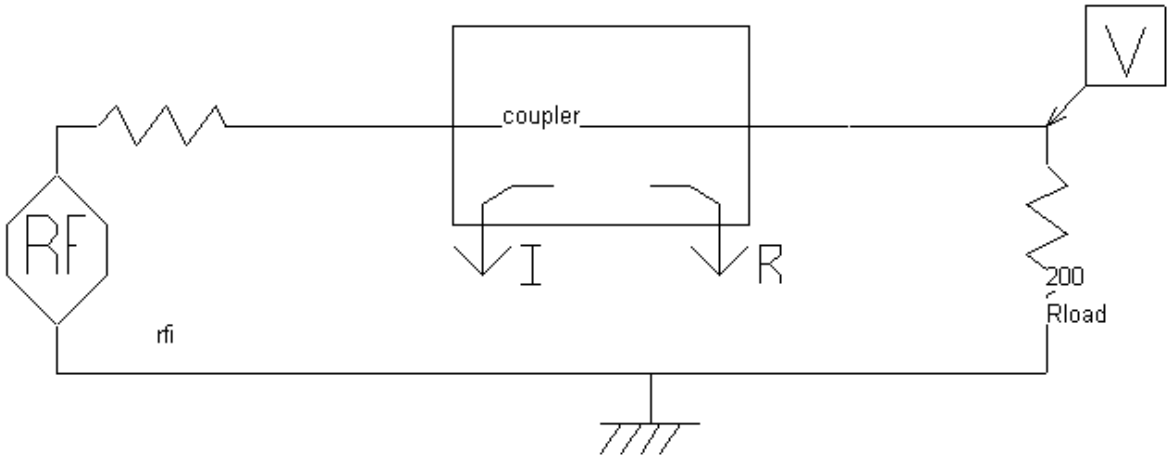
Class	Limit @ 100 MHz
1	42 dB µV/m
2	36 dB µV/m
3	30 dB µV/m
4	24 dB µV/m
5	18 dB µV/m

Synthesis of Exercises 1 to 8

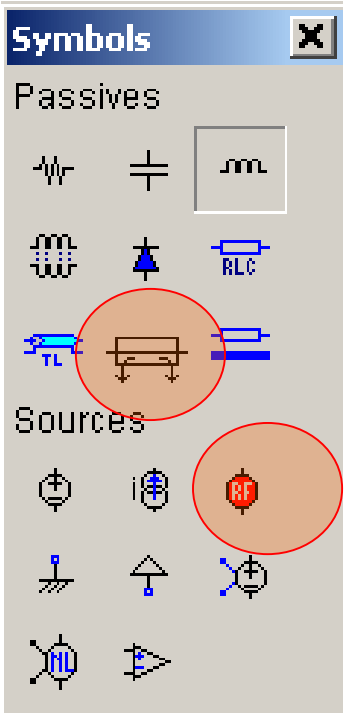
- **What did we learn ?**

Exercise 10. Estimation of susceptibility level

– A RF generator produces a conducted disturbance which is injected on a 200 Ω load, though a directional coupler.



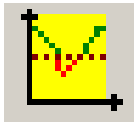
Ex9-RloadSusc.sch

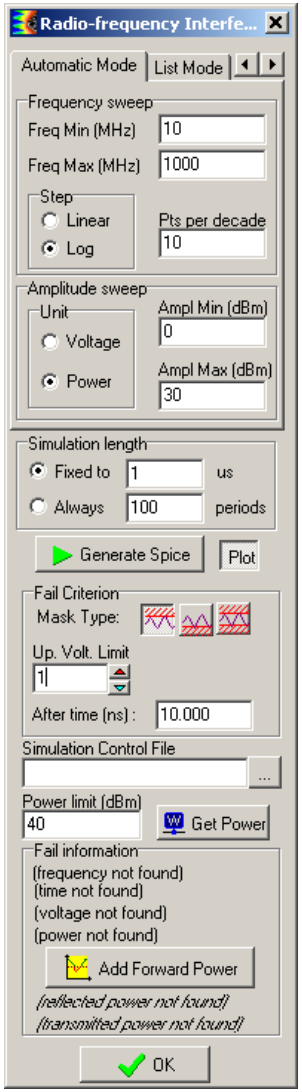


– Estimate the forward power to induce 1 V across the load over the frequency range 10 MHz – 1 GHz.

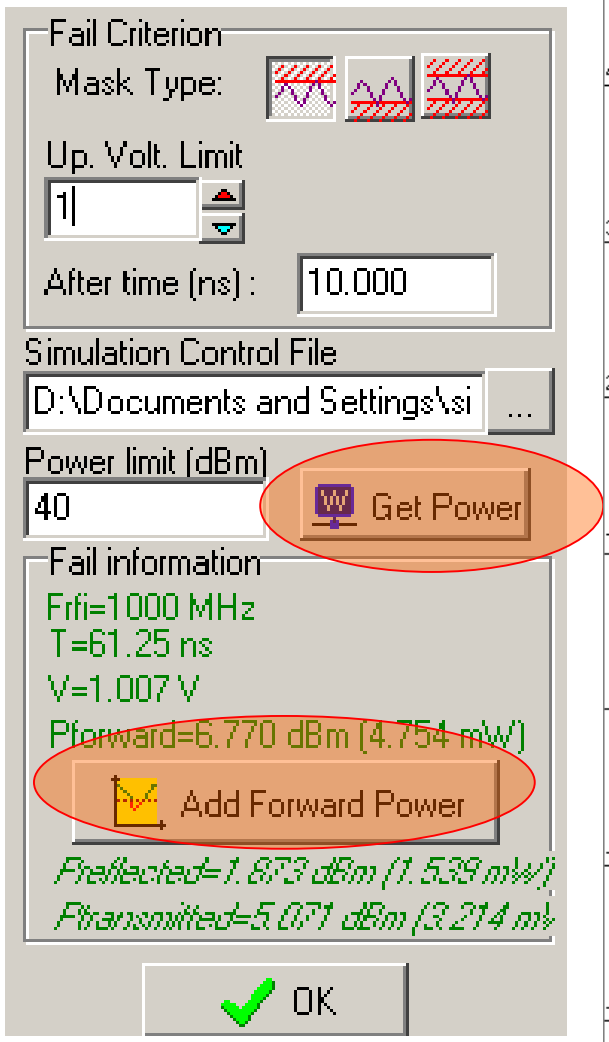
Exercise 10. Estimation of susceptibility level

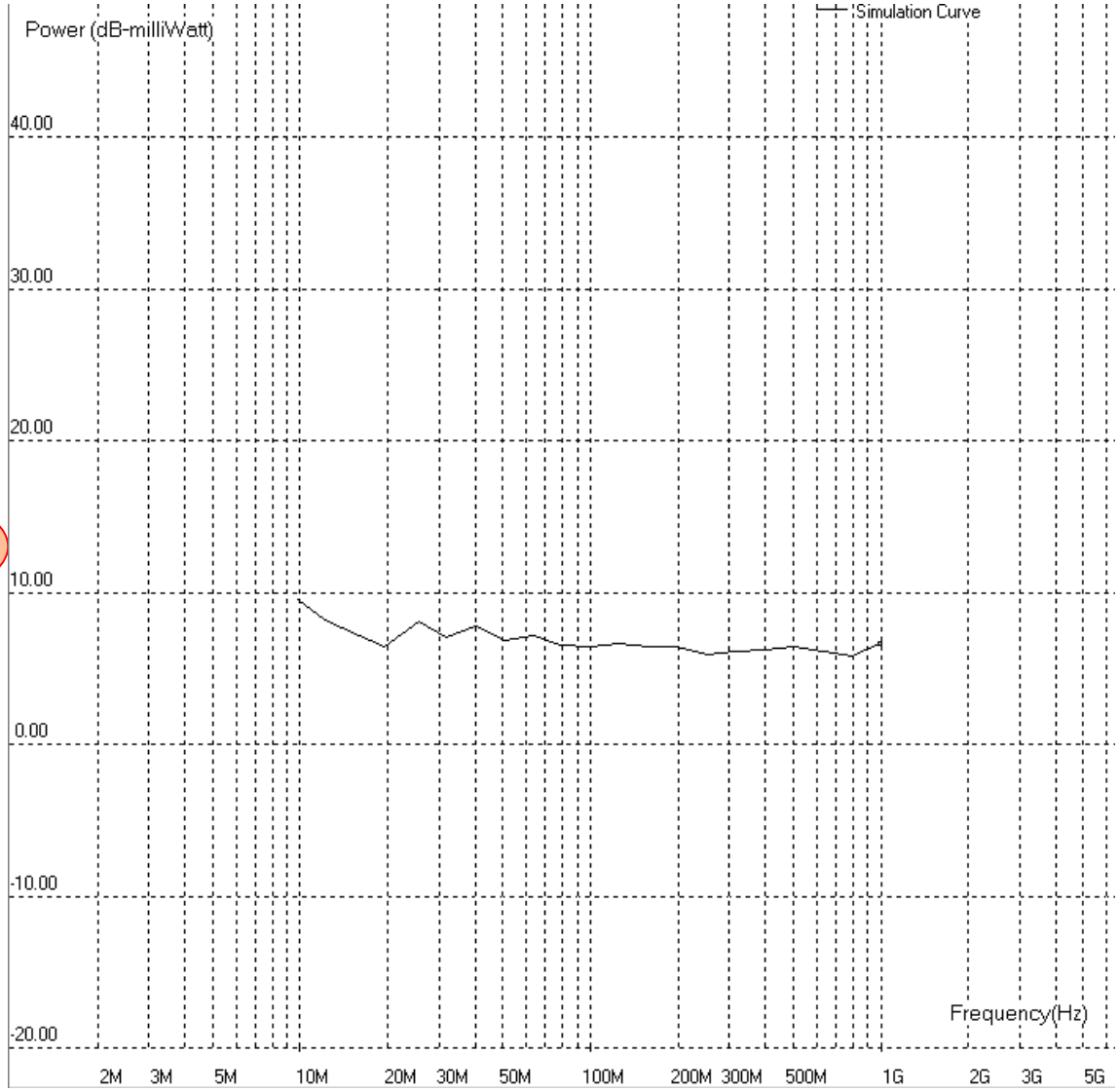
- Launch Susceptibility tool
- Configure the RF disturbance and launch SPICE simulation
- Configure the voltage criterion and extract susceptibility threshold
- Display the susceptibility threshold



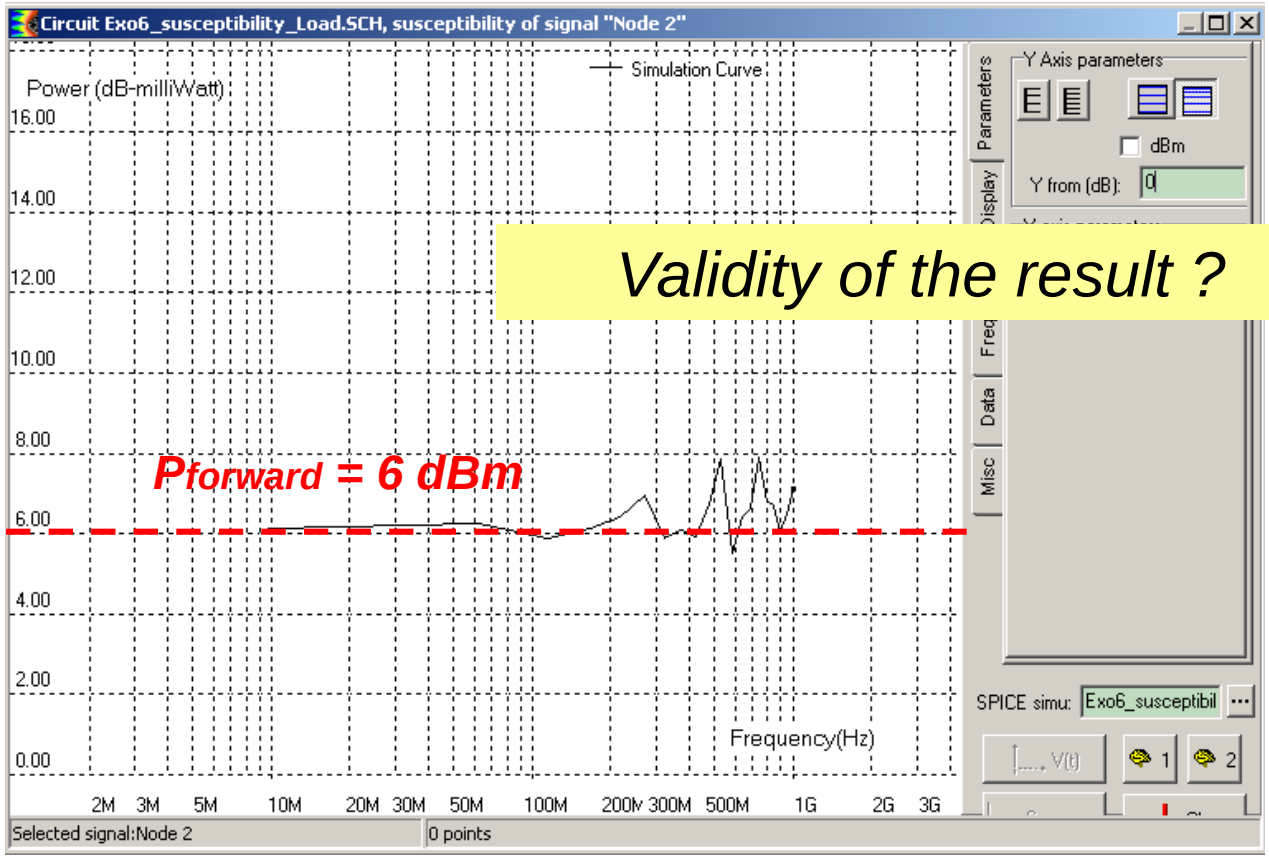


Exercise 10. Estimation of susceptibility level





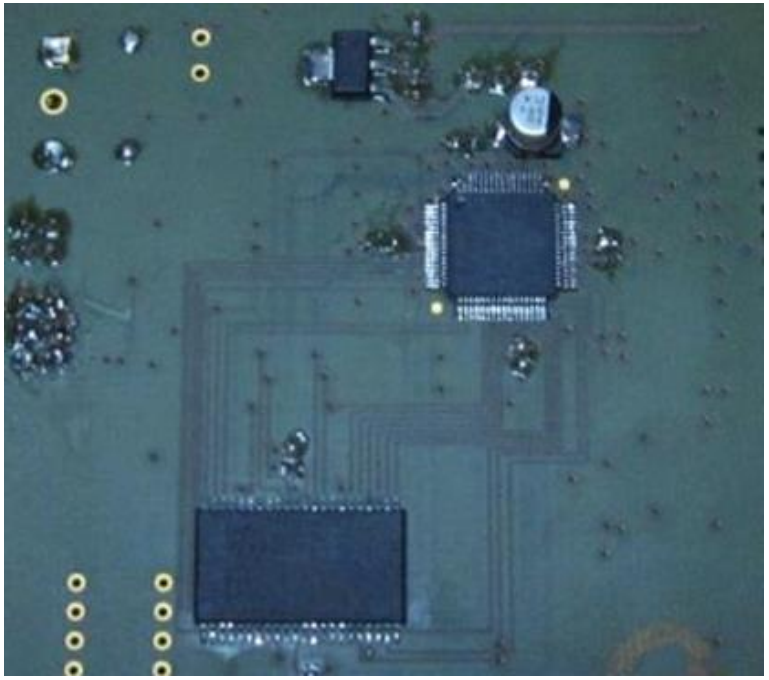
Exercise 10. Estimation of susceptibility level



Validity of the result ?

Exercise 11. Susceptibility of analog input

- A RF disturbance is conducted to an analog input.
- DPI: 1 nF
- PCB: short tracks
- Equivalent model: see IBIS.
- Susceptibility criterion : input noise < 100 mV from 10 MHz to 1 GHz.



Ex10-ADCInputSusc.sch

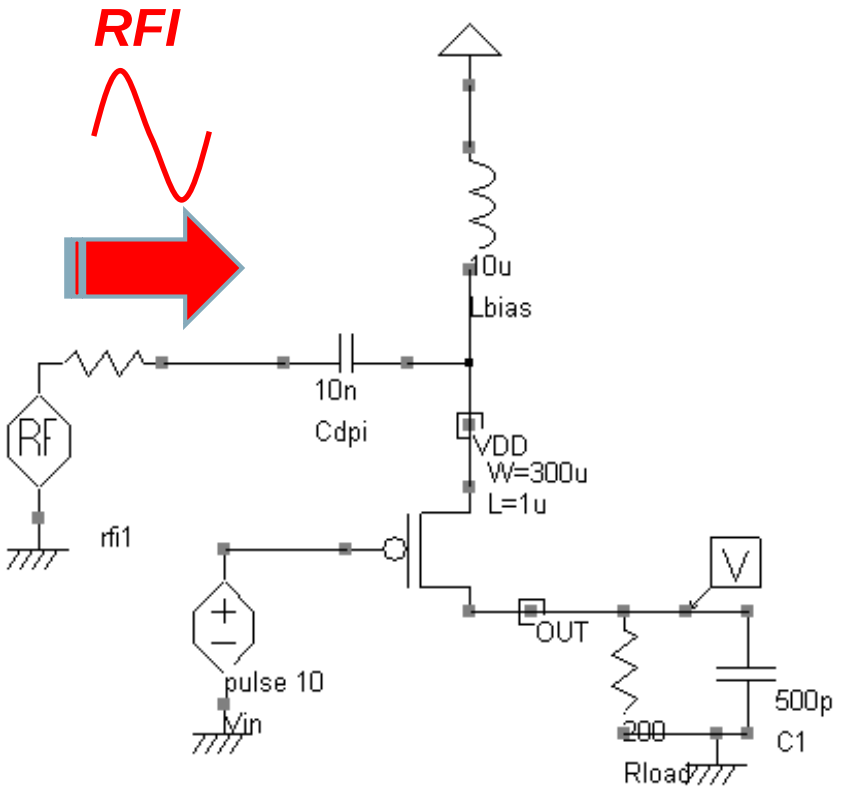
Exercise 12. Susceptibility of output buffer

– The following output is loaded by a 200 Ω load and a 0.5 nF capacitance.

– The susceptibility of the buffer is tested using DPI standard.

– Harmonic disturbances are injected on power supply

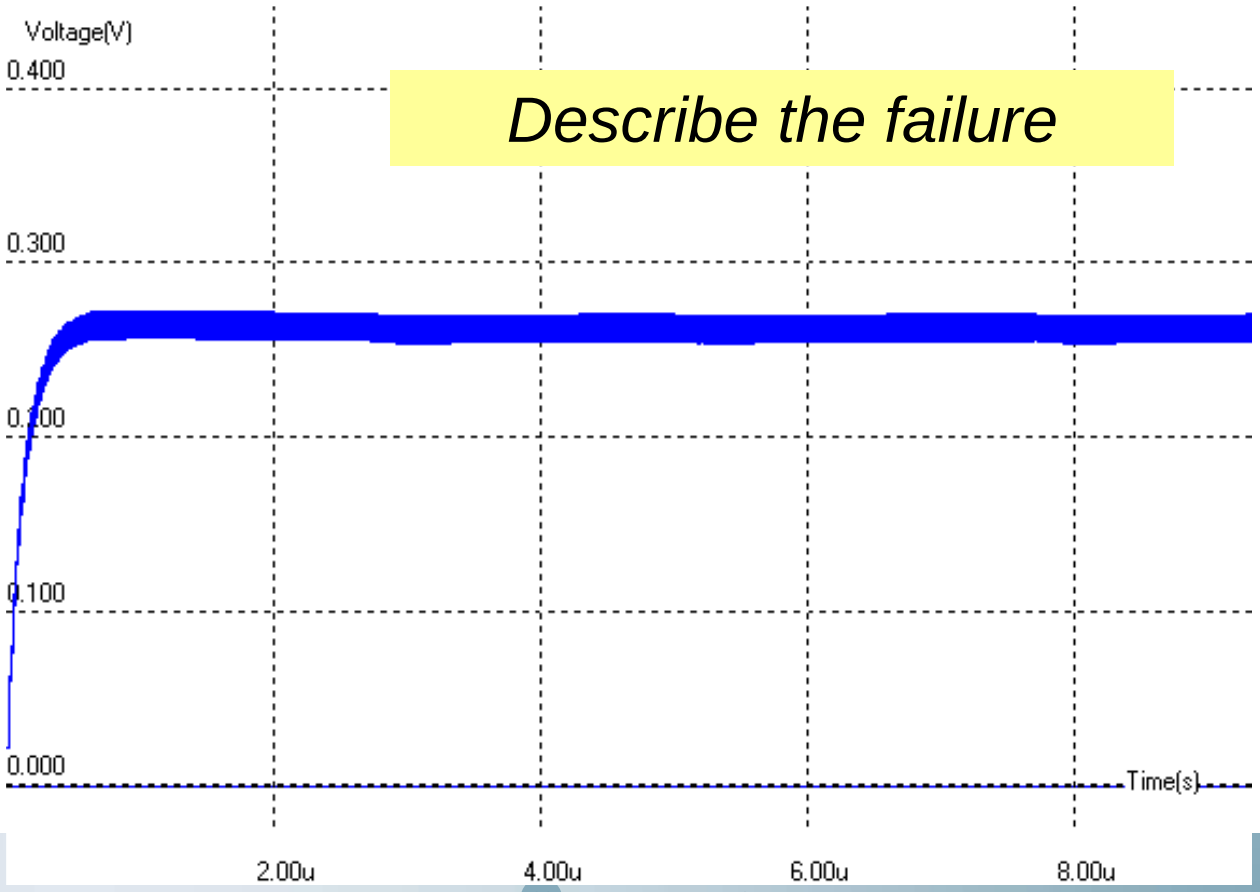
Susceptibility criterion ?



Ex11-HighSideEMI.sch

Exercise 12. Susceptibility of output buffer

- Injection on the Vdd pin
- Add a 100 MHz RFI sinus signal with 2 V amplitude.



Describe the failure

Exercise 12. Susceptibility of output buffer

- Failure due to rectification effect.
- Equation of drain current based on MOS Model 1:

$$\mathrm{Ids} = \frac{\beta}{2}(V_{GS} - V_T)^2(1 + \lambda.V_{DS})$$

Square function → Non linear behavior

Synthesis of Exercises 9 to 12

- **What did we learn?**

Thank you for your attention