EMC of integrated circuits

Lab –Prediction of the immunity of a CAN bus

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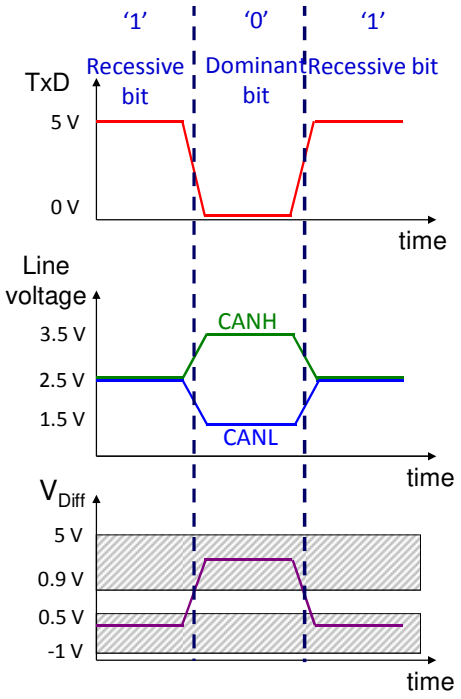
The bus Controller Area Network (CAN) is a serial digital bus widely used in automotive systems. It is dedicated to the communications between the different equipments in a vehicle. The bus was proposed by Bosch as real-time communication protocol for distributed systems. It withstands a maximum data rate of 1 Mbits/s and satisfies numerous requirements in term of robustness and fault tolerances. It was standardized in 1991 as IEC11898. Fig. 1 presents the hardware architecture of this bus, made of three main parts:

- the CAN controller which manages the access to the transmission medium, the frame construction, the error detection. It is usually embedded within a microcontroller. It has two physical pins TxD and RxD for the transmission and the reception of messages.
- the CAN transceiver CAN which ensures the physical interface with the transmission medium
- the transmission medium, usually a 120 Ω +/- 10 Ω twisted-wire pair (TWP). Both wires are called CANH and CANL and they form a differential pair. The transmitted logical state depends on the differential voltage $V_{Diff} = V_{CANH}-V_{CANL}$.

In order to prevent any collisions when two nodes try to transmit simultaneously, the bus access is based on Carrier Sense Multiple Access/Bitwise Arbitration (CSMA/BA). A priority level is assigned to each message during an arbitration phase. The priority is based on the difference of weight of binary states: state '0' is the dominant state (it forces the electrical state of the bus) while state '1' is the recessive state. The recessive state is the default state of the bus. During the arbitration phase, a node stops any communication if it senses a dominant state on the bus. The output of its transceiver becomes recessive and it stays in reception mode. In recessive state, V_{Diff} is less than 0.5 V. In dominant state, V_{Diff} is greater than 2 V . Generally, V_{Diff} is equal to 2 V in dominant state and to 0 V in recessive state. Moreover, the common-mode voltage of the bus must range between -12 V and + 12 V.



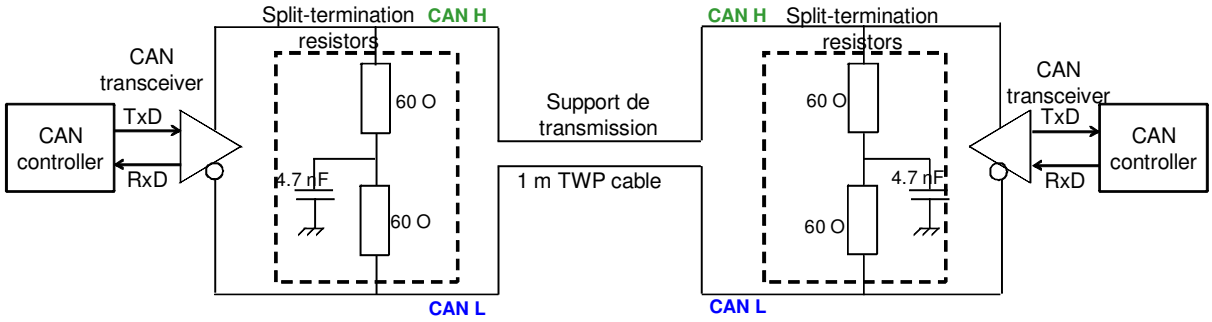


Fig. 1 - Hardware architecture of a CAN bus

As CAN transceivers are directly connected to a long cable harness, they must meet stringent RF susceptibility requirements. The figure above shows a common conducted disturbance injection set-up for a CAN bus based on the IEC 62132-4 Direct Power Injection (DPI) standard. During conducted susceptibility tests, CAN communication has to remain unaffected by harmonic disturbances between 150 kHz and 1 GHz with a forward power limit set at 30 dBm.

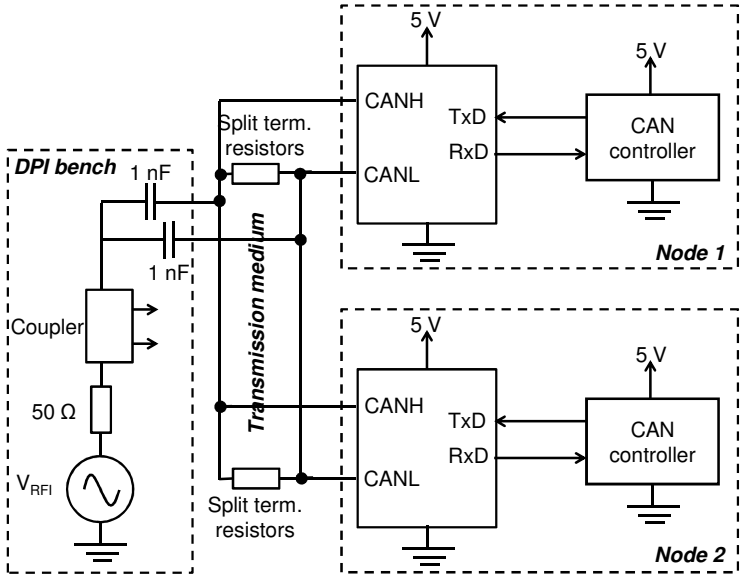


Fig. 2 - Conducted susceptibility test set-up on CAN transceiver (according to DPI standard)

The objective of this exercise is to model the conducted RF injection into a CAN bus driven by two different versions of CAN transceivers and to predict their susceptibility levels. The two versions are called version A and version B. Their input impedances have been characterised for both logical states. The measurement results are shown in the figure below. Moreover, CANH and CANL pins are internally protected by diodes triggered at +/- 30 V. They are not supposed to trigger during the conducted susceptibility test. In the following part, the influence of the transmission medium (usually a twisted-wire pair cable) will be neglected for simplification purpose.

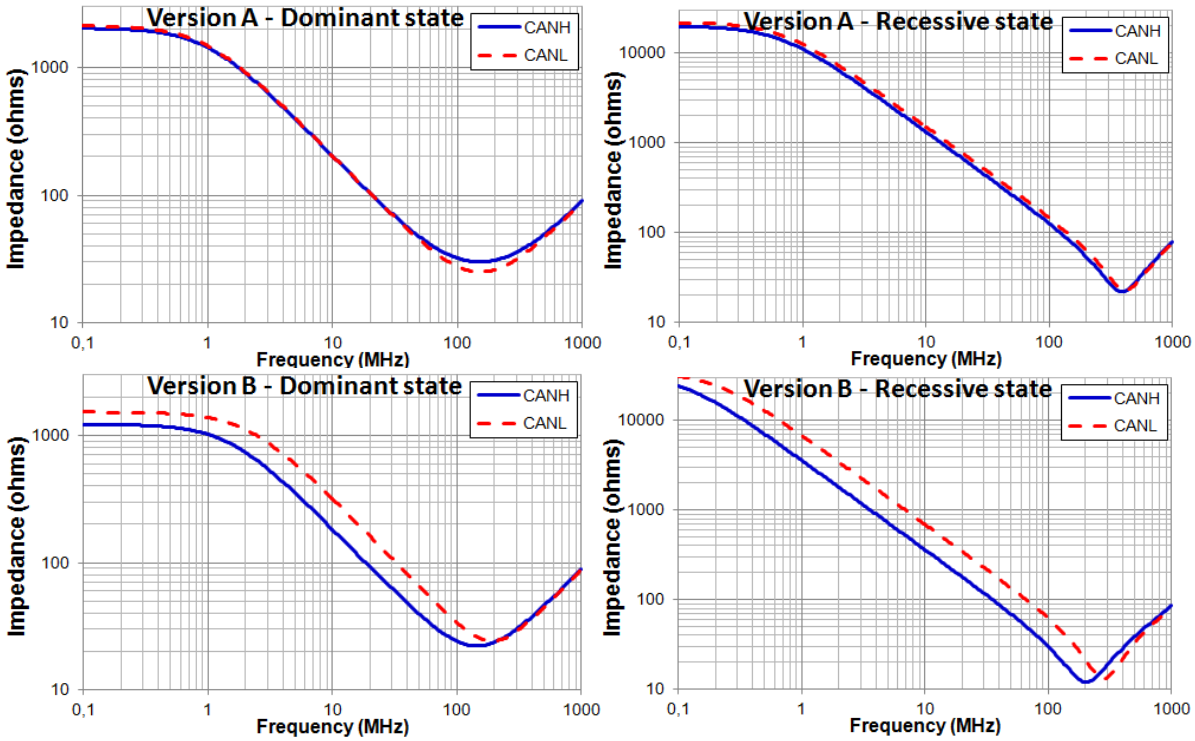


Fig. 3 - Input impedance of CANH/CANL pins of CAN transceivers version A and B, in dominant or recessive states

1. Is the transmission of a dominant bit carried out in common-mode or differential mode ?

2. Is the conducted injection carried out in common mode or differential mode? Why is it a representative injection mode for a practical situation?

3. What is the purpose of 60 Ω resistors of the device "split-termination resistors" ? Why is it advised to add a capacitor? Why is 4.7 nF an appropriate value?

4. What happen if the amplitude of the voltages induced on terminations of CANH and CANL lines exceeds 12 V ? Same question if the differential voltage V_{Diff} exceeds 0.4 V ? Is the bus sensitive to common-mode noise ? To differential mode noise ?

5. Initially, we neglect the actual electrical model of the CAN transceiver. It is supposed to be an infinite impedance. Build the electrical model of the DPI injection on the CAN bus.

6. Simulate the common-mode voltage ( ) and differential-mode voltage ( ) induced on bus terminations for maximum injection level. Fill the table below. What type(s) of failures may arise? Why ?

Frequency	*Common-mode voltage amplitude (V)*	*Differential-mode voltage amplitude (V)*
1 MHz		
3 MHz		
10 MHz		
30 MHz		
100 MHz		
400 MHz		

7. The termination resistors are given with a tolerance of +/- 5 Ω. Repeat question 7 in the worst case situation.

8. Propose a first general rule for the design of a robust CAN bus to electromagnetic disturbance.

9. Now, the actual electrical model of CAN transceiver will be considered. Is it possible for the outputs of two nodes connected to the same bus to be in the same logic state?

10. From the impedance measurements taken on the CAN transceiver (versions A and B), build equivalent electrical models of pins CANH and CANL in recessive and dominant state.

11. In the next parts, we consider the case where a recessive state is transmitted. The models are initially used to predict whether the internal protection diodes will trigger during the conducted injection test.

a. Build the electrical models to detect this type of failure with both transceiver versions.

b. Simulate the susceptibility level of this type of failure for both transceiver types. Are the protection diodes likely to trigger during the conducted susceptibility test?

12. The models are then used to predict transmission errors due to bit flipping (misinterpretation of the binary state by the receiving node).

a. Modify the previous electrical model to detect this type of failure with both transceiver versions.

b. Simulate the susceptibility level of this type of failure for both transceiver types. Is the risk of communication error due electromagnetic disturbance negligible for transceiver version A? What about transceiver version B?

9. Explain the difference in susceptibility between both versions of the CAN transceiver. What recommendation could you give a designer wishing to make a robust CAN transceiver that withstands electromagnetic disturbance?

Annex – Susceptibility analysis tool

IC-EMC proposes a tool for the analysis of susceptibility of components to harmonic disturbance. It is available in the menu 'EMC > Susceptibility analysis' or with the icon  . Its purpose is twofold: build SPICE model with all the parameters for susceptibility simulation, and a post-processing tool of the simulation results. The simulation is based on a transient simulation.

The figure below presents the simulation flow of the tool. The electrical model of the device under test has been constructed and validated previously. A specific harmonic disturbance generator, called RFI source  , whose amplitude increases linearly with time, is integrated to the model. It also includes a coupler  in order to extract the forward power delivered by the RFI source. The susceptibility analysis tool is used to set the RFI source frequency and amplitude sweep parameters. The model of SPICE netlist is then built and simulated by WinSPICE. At the end of the SPICE simulation, the tool analyzes the output results, detects failures and extracts the required forward power to trigger this failure.

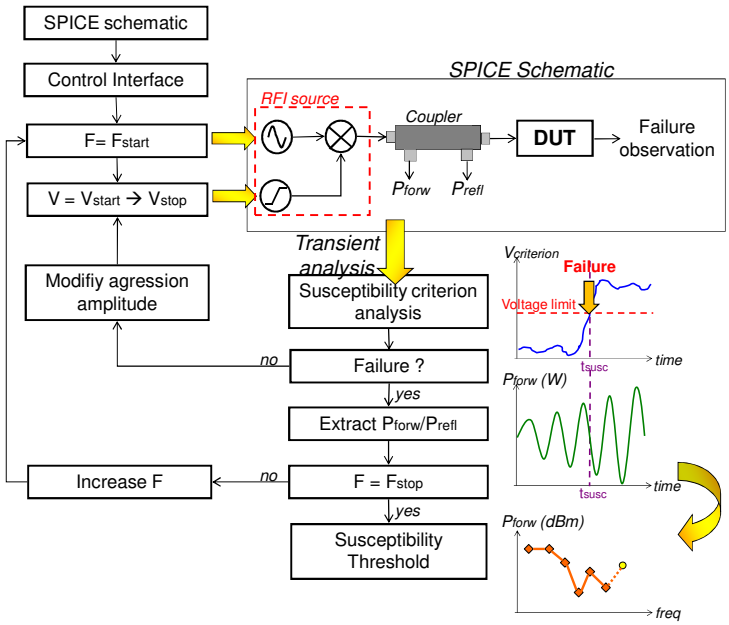


Fig. 4 - Simulation flow of the susceptibility analysis tool of IC-EMC

Fig. 5 presents the interface of the tool. Three simulation modes are proposed:

- manual mode: the user configures the simulation only for one disturbance frequency. Only the amplitude of the RFI source is increased during the simulation in order to find the susceptibility threshold at this frequency. This mode is advised to get familiar with this tool.
- automatic mode: the user configures several transient simulations at different disturbance frequencies. The frequency sweep is linear or logarithmic. For each frequency, the RFI source amplitude is swept in order to determine the susceptibility threshold.
- List mode: same principle than in automatic model, but the frequency and amplitude sweeps are defined in a text file.

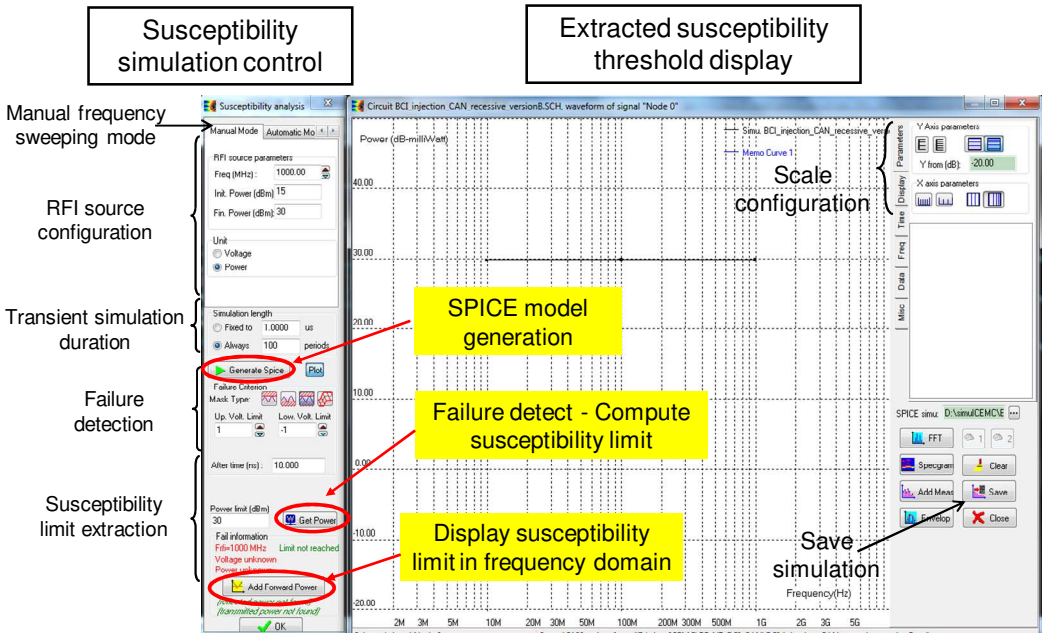


Fig. 5 - Interface of the susceptibility analysis tool (manual mode)

In manual mode, the user defines the frequency of the disturbance produced by the RFI source, its amplitude sweep (in voltage (V) or power (dBm)) and the duration of the simulation (expressed in µs or in number of harmonic disturbance period). The parameters of the RFI source are shown in Fig. 6. Then, Click on the button 'Generate SPICE' to launch the transient simulation. WinSPICE must be opened before. At the end of the simulation, define the Failure Criterion and click on the button 'Get Power' to detect a failure and extract the forward power. To save this point, click on the button 'Add Forward Power'.

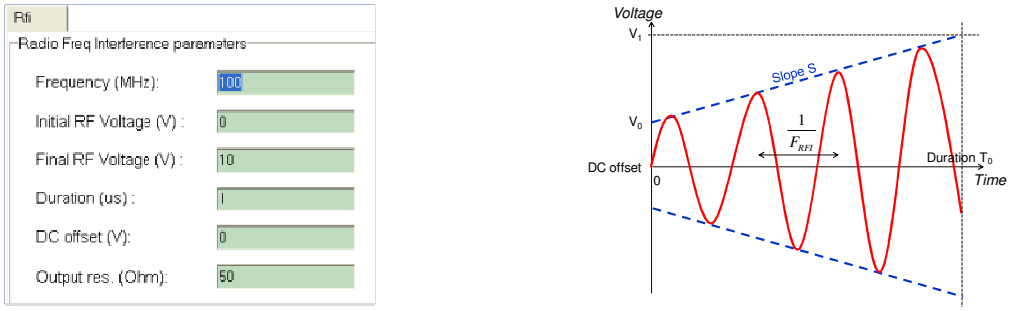


Fig. 6 - RFI source parameters

Failures are not detected during the SPICE simulation, but by the post-processing tool. The detected failure depends on the failure criterion. The detection method consists in an analysis of the simulation electrical signal (voltage or current) and detect the time it exceeds a predefined limit. The simplest method consists in verifying that the signal does not exceed a margin amplitude, as described in Fig. 7. For example, the figure shows the disturbance of a voltage reference equal nominally to 2.5 V. The following failure criterion is defined: the voltage reference should not vary of more than 20 % of the nominal voltage. Thus the maximum fluctuation is equal to 500 mV. In IC-EMC, the failure criterion is defined as follows: the reference voltage is monitored. The upper and lower limit of this voltage are defined by clicking on the button  , and filling the fields 'Up Volt with

3 and 2 respectively. If the reference voltage goes beyond the limit 'Up Volt. Limit' or below the limit 'Low Volt. Limit', then a failure is detected and the tool computes the forward power of the disturbance that leads to this failure.

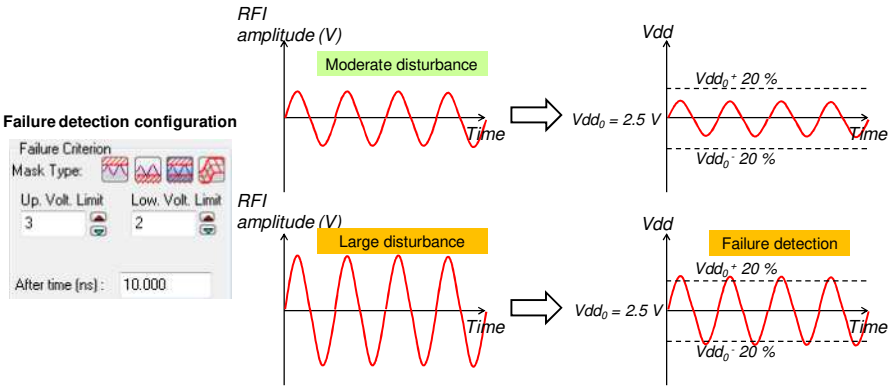


Fig. 7 - Failure criterion definition