EMC of integrated circuits

Lab – BCI virtual test bench and prediction of the immunity of a CAN bus

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I. General presentation of the lab

The method Bulk Current Injection (BCI) is usually employed to qualify the immunity of electronic equipments and components to electromagnetic radiofrequency disturbance. This method is proposed in several standards such as:

- ISO11452-4 for the test of automotive electronic equipments
- DO-160G section 20 for the test of avionic electronic equipments
- IEC62132-3 for the test of bus interface circuits

The method consists in a conducted injection of current along cable, that reproduces the effect of the coupling of a radiation on a cable in a simple and compact way. The injection is done by a shielded clamp (Fig. 1), that forms a transformer with the cable. The coupling is inductive, the capacitive coupling is suppressed by the clamp shielding.

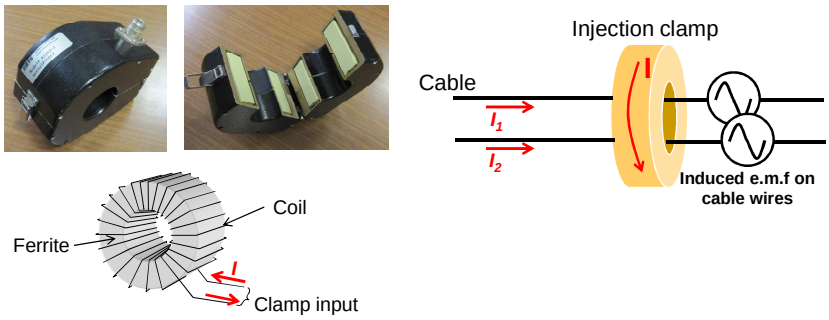


Fig. 1 - BCI clamp and principle of the injection

Fig. 2 presents a typical BCI test bench. A harmonic disturbance with a frequency between 1 and 400 MHz is produced by a signal synthesizer and amplified by a 50 W power amplifier. The forward power is measured with a directional coupler and a powermeter. The injection clamp is placed around a cable, which is routed at 5 cm above a reference ground plane. During the immunity test, the operation of the component under test is checked in order to detect a failure. The test aims at determining at each frequency of the disturbance the induced current required to induce a functional failure of the component under test.

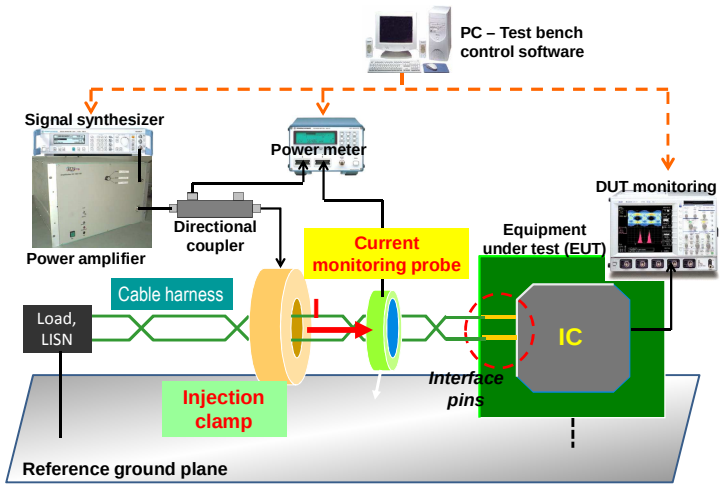


Fig. 2 - BCI test bench

The BCI standard BCI proposes two test modes:

- Open-loop configuration: the current induced on the cable is not measured directly. It is deduced from the measurement of the forward power and a calibration of the injection clamp.
- Closed-loop configuration: a current probe is placed on the cable to read in real time the current induced on the cable.

Depending on the used standard, the maximum injected current level that the component under test may vary. The following table gives the maximum current defined by the standard IEC62132-3 for interface circuits.

Test severity level	Current limit
I	50 mA
II	100 mA
III	200 mA
IV	300 mA
V	Specific value agreed between the users of this standard

The objective of this lab is the development of an electrical model of the BCI test bench in open-loop configuration in order to predict the compliance of the component under test to the immunity limit defined by the standard. This test bench will be used to evaluate the immunity of several interface components for CAN bus, called CAN transceiver, and select the more robust to electromagnetic disturbance. These devices must withstand the severity level IV. The models will be built with IC-EMC and simulated with WinSPICE.

The lab is divided in three parts with questions to help you to build models and analyze the simulation results. You will provide a report at the end of the lab with the answers to the different questions.

II. Part 1 - Calibration of a BCI test bench in open-loop configuration

The objective of this first part is the development of the model of the BCI test bench and the computation of the injection power required to induce a given current on the cable under test.

The BCI test bench uses an open-loop configuration. A calibration is required to relate the power delivered by the amplifier and the induced current. The calibration uses a device called calibration jig shown in Fig. 3. It is a 50 Ω matched short transmission line. The injection clamp is placed around the jig and is excited by a harmonic signal whose delivered power is measured. The jig is terminated by a 50 Ω load and a measurement receiver at the other side. The receiver measures the induced current on the jig. Therefore, it is possible to relate injection source voltage, delivered power and the induced current on a cable by the injection clamp. The coupling between the clamp and any cable is supposed to be the same that the coupling between the clamp and the jig.

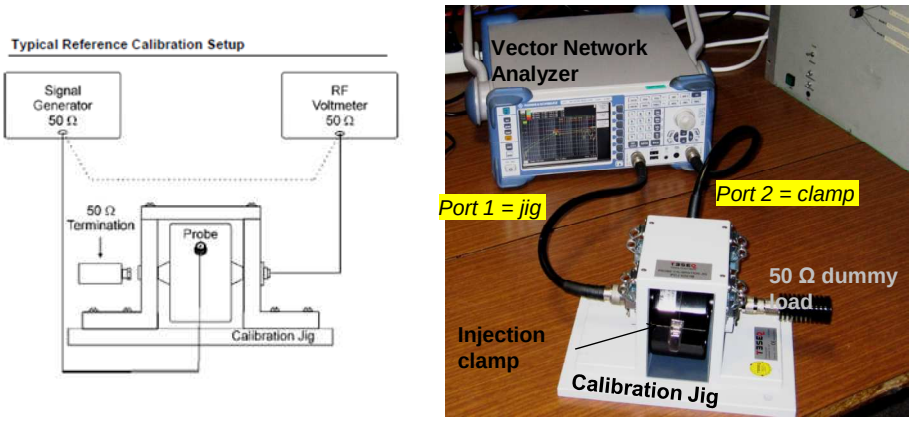
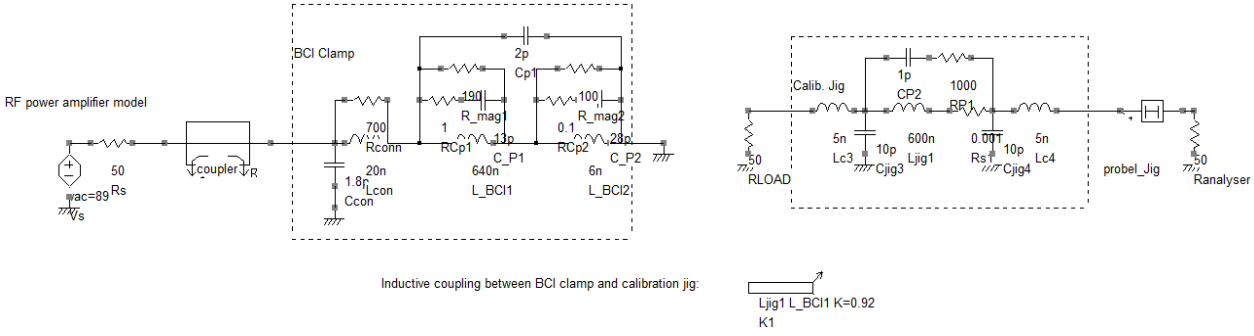


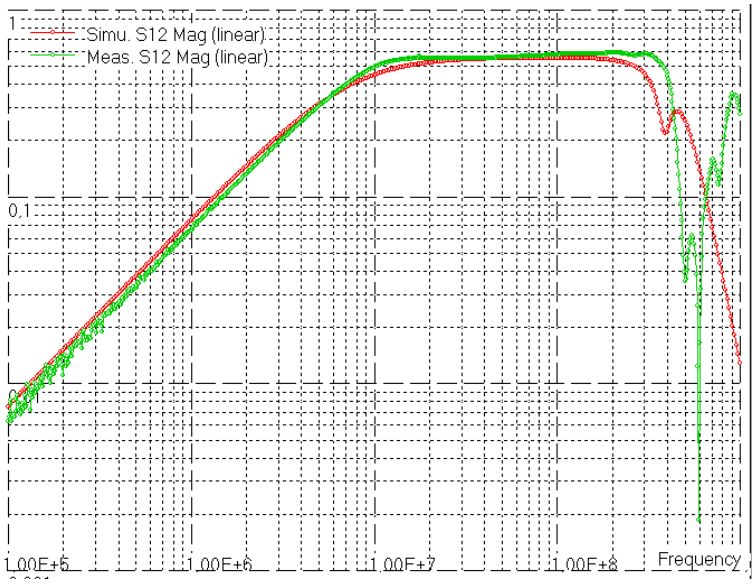
Fig. 3 - Calibration jig and calibration of the BCI injection clamp

The following figure presents an electrical model for the simulation of the coupling between the injection clamp and the calibration jig. The inductive coupling is given by a mutual coupling coefficient K1, according to the following equation:

$$K = \frac{M_{12}}{\sqrt{L_1 \times L_2}}$$

where L1 and L2 are the two coupled inductances and M12 the mutual inductance. K ranges from 0 (lack of inductive coupling) to 1 (ideal coupling). This model is available in the file Clamp_coupling_calib_jig.sch. The comparison between measurements and simulations of the transmission coefficient between the clamp and the jig is shown below.





1. Comment the evolution of the coupling between the injection clamp and the jig in frequency domain.

2. Build an electrical model to simulate the calibration of the BCI test bench in open-loop configuration. Place a coupler (symbol) in order to extract the forward power and a current probe (symbol) to extract the induced current on the jig.

3. With this model, evaluate the voltage amplitude of the excitation soruce and the required forward power to induce 300 mA on the calibration jig. Fill the table below. You can use the susceptibility analysis tool of IC-EMC (see annex at the end of the document).

Frequency	*RF generator voltage (V)*	*Forward power required to induce 300 mA (dBm)*	*Max. forward power during BCI test (dBm)*
1 MHz			
3 MHz			
10 MHz			
30 MHz			
100 MHz			
400 MHz			

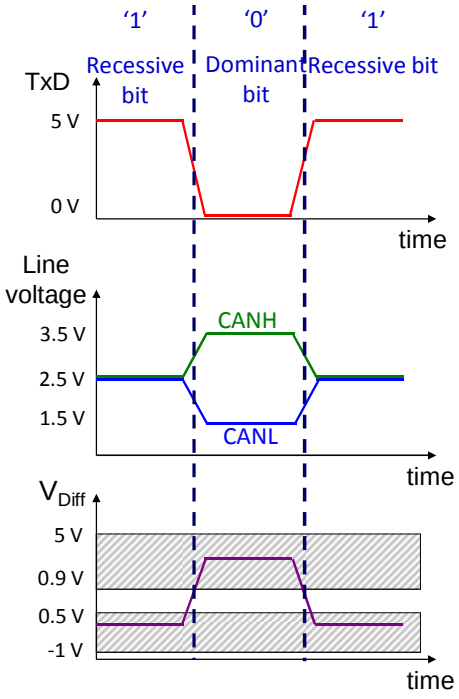
III. Part 2 - Simulation of the susceptibility of a generic CAN bus

The objective of this second part is the construction of a basic CAN bus and the BCI injection. Firstly, no specific transceiver will be considered. A realistic model of a CAN transceiver will be included in the third part.

The bus Controller Area Network (CAN) is a serial digital bus widely used in automotive systems. It is dedicated to the communications between the different equipments in a vehicle. The bus was proposed by Bosch as real-time communication protocol for distributed systems. It withstands a maximum data rate of 1 Mbits/s and satisfies numerous requirements in term of robustness and fault tolerances. It was standardized in 1991 as IEC11898. Fig. 4 presents the hardware architecture of this bus, made of three main parts:

- the CAN controller which manages the access to the transmission medium, the frame construction, the error detection. It is usually embedded within a microcontroller. It has two physical pins TxD and RxD for the transmission and the reception of messages.
- the CAN transceiver CAN which ensures the physical interface with the transmission medium
- the transmission medium, usually a 120 Ω +/- 10 Ω twisted-wire pair (TWP). Both wires are called CANH and CANL and they form a differential pair. The transmitted logical state depends on the differential voltage $V_{Diff} = V_{CANH}-V_{CANL}$.

In order to prevent any collisions when two nodes try to transmit simultaneously, the bus access is based on Carrier Sense Multiple Access/Bitwise Arbitration (CSMA/BA). A priority level is assigned to each message during an arbitration phase. The priority is based on the difference of weight of binary states: state '0' is the dominant state (it forces the electrical state of the bus) while state '1' is the recessive state. The recessive state is the default state of the bus. During the arbitration phase, a node stops any communication if it senses a dominant state on the bus. The output of its transceiver becomes recessive and it stays in reception mode. In recessive state, V_{Diff} is less than 0.5 V. In dominant state, V_{Diff} is greater than 2 V . Generally, V_{Diff} is equal to 2 V in dominant state and to 0 V in recessive state. Moreover, the common-mode voltage of the bus must range between -12 V and + 12 V.



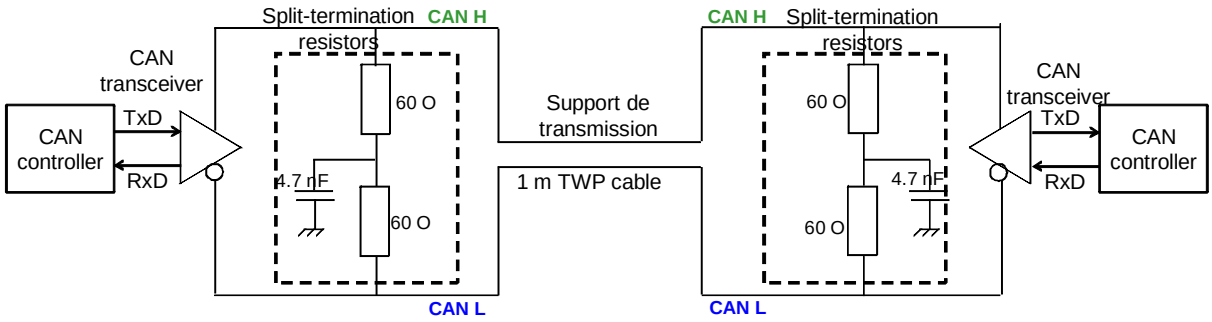


Fig. 4 - Hardware architecture of a CAN bus

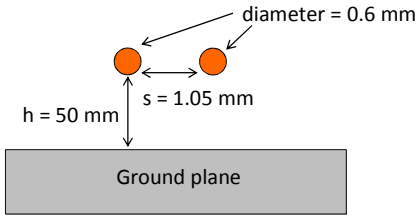
In the following parts, the transmission medium is considered as a 1 m long TWP, placed at 5 cm of a reference ground plane.

4.What is the direction of the current during the transmission of a dominant bit ? During the BCI test, what is the direction of the current induced on both wires of the TWP. In both cases, what is the nature of the current ?

5. What is the purpose of 60 Ω resistors of the device "split-termination resistors" ? Why is it advised to add a capacitor? Why is 4.7 nF an appropriate value?

6. What happen if the amplitude of the voltages induced on terminations of CANH and CANL lines exceeds 12 V ? Same question if the differential voltage V_{Diff} exceeds 0.4 V ? Is the bus sensitive to common-mode voltage ? To differential mode voltage ?

7. The following figure presents a cross-section of the TWP cable. With the tool 'Tools/Cable modeling', check that this cable satisfies for CAN Bus. Build an equivalent electrical model valid up to 400 MHz.



8. Build the electrical model of the BCI injection on the CAN bus. The CAN transceiver is supposed ideal, CANH and CANL pin impedance are considered as infinite. The injection clamp is placed in the middle of the TWP cable.

9. Simulate the common-mode voltage ( ) and differential-mode voltage ( ) induced on bus terminations for maximum injection level. Fill the table below. What type(s) of failures may arise? Why ?

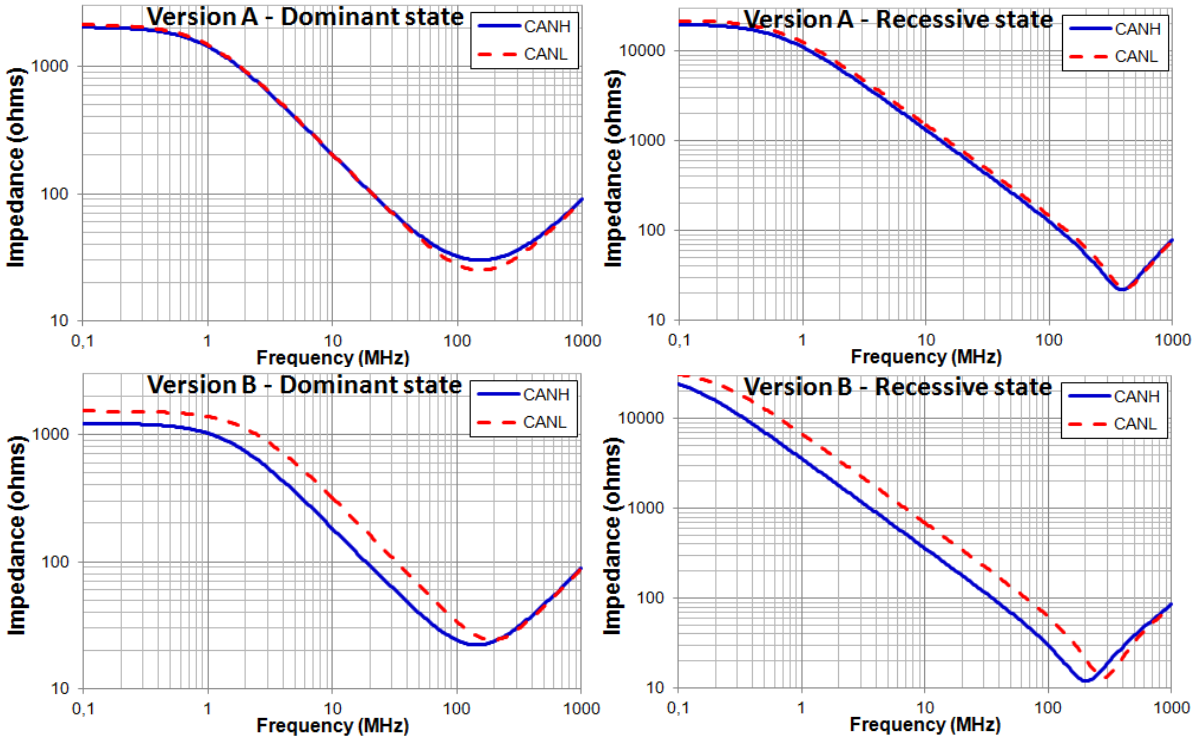
Frequency	*Common-mode voltage amplitude (V)*	*Differential-mode voltage amplitude (V)*
1 MHz		
3 MHz		
10 MHz		
30 MHz		
100 MHz		
400 MHz		

10. The termination resistors are given with a tolerance of +/- 5 Ω. Do question 9 in the worst case situation.

11. Propose a general rule for the design of a robust CAN bus to electromagnetic disturbance.

IV. Part 3 - Selection of a CAN transceiver

In the third part, a realistic model of the CAN transceiver is considered. The objective is the prediction of the susceptibility with two different versions of CAN transceivers, named versions A and B. The impedances of their pins CANH and CANL have been measured in dominant and recessive states.



12. Is it possible for two transceivers to have their outputs in the same state ?

13. From the impedance measurement results shown above, build electrical models of CANH and CANL in recessive and dominant states, for versions A and B.

14. Add the transceiver models to the BCI test bench model built in part 2. The termination resistors are supposed perfectly balanced. We consider the transmission of a recessive state.

15. We want to simulate a reception error during a BCI injection. Propose a method to detect this type of error.

16. Simulate the susceptibility level of each transceiver version for this type of failure. Should we neglect the reception errors due to electromagnetic disturbance with CAN transceiver version A ? with version B ?

17. Explain the difference of susceptibility level between both transceivers? Which recommendation could you propose to designers of CAN transceiver to make them more robust to electromagnetic disturbance?

V. Annex – Susceptibility analysis tool

IC-EMC proposes a tool for the analysis of susceptibility of components to harmonic disturbance. It is available in the menu 'EMC > Susceptibility analysis' or with the icon  . Its purpose is twofold: build SPICE model with all the parameters for susceptibility simulation, and a post-processing tool of the simulation results. The simulation is based on a transient simulation.

The figure below presents the simulation flow of the tool. The electrical model of the device under test has been constructed and validated previously. A specific harmonic disturbance generator, called RFI source  , whose amplitude increases linearly with time, is integrated to the model. It also includes a coupler  in order to extract the forward power delivered by the RFI source. The susceptibility analysis tool is used to set the RFI source frequency and amplitude sweep parameters. The model of SPICE netlist is then built and simulated by WinSPICE. At the end of the SPICE simulation, the tool analyzes the output results, detects failures and extracts the required forward power to trigger this failure.

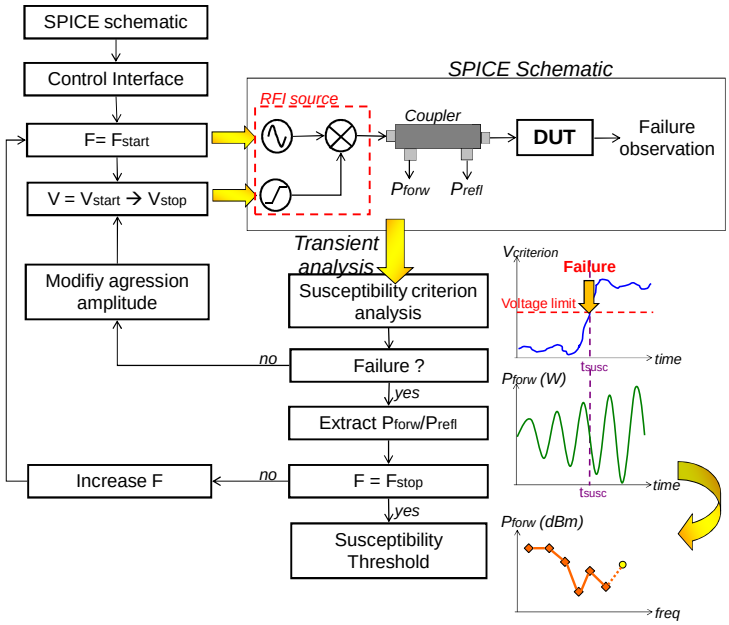


Fig. 5 - Simulation flow of the susceptibility analysis tool of IC-EMC

Fig. 6 presents the interface of the tool. Three simulation modes are proposed:

- manual mode: the user configures the simulation only for one disturbance frequency. Only the amplitude of the RFI source is increased during the simulation in order to find the susceptibility threshold at this frequency. This mode is advised to get familiar with this tool.
- automatic mode: the user configures several transient simulations at different disturbance frequencies. The frequency sweep is linear or logarithmic. For each frequency, the RFI source amplitude is swept in order to determine the susceptibility threshold.

- List mode: same principle than in automatic model, but the frequency and amplitude sweeps are defined in a text file.

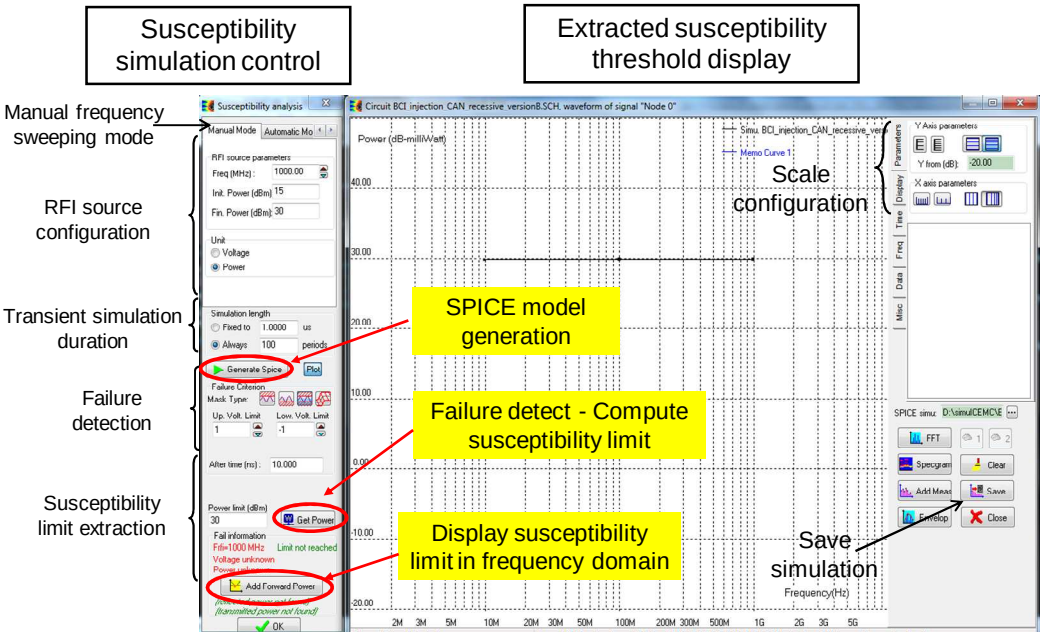


Fig. 6 - Interface of the susceptibility analysis tool (manual mode)

In manual mode, the user defines the frequency of the disturbance produced by the RFI source, its amplitude sweep (in voltage (V) or power (dBm)) and the duration of the simulation (expressed in µs or in number of harmonic disturbance period). The parameters of the RFI source are shown in Fig. 7. Then, Click on the button 'Generate SPICE' to launch the transient simulation. WinSPICE must be opened before. At the end of the simulation, define the Failure Criterion and click on the button 'Get Power' to detect a failure and extract the forward power. To save this point, click on the button 'Add Forward Power'.

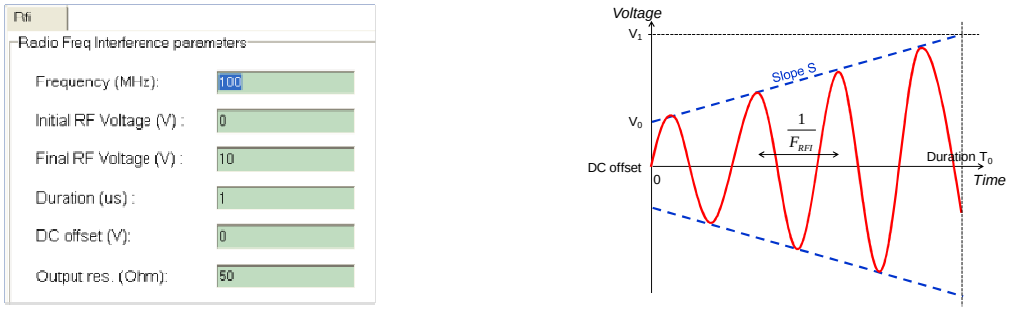


Fig. 7 - RFI source parameters

Failures are not detected during the SPICE simulation, but by the post-processing tool. The detected failure depends on the failure criterion. The detection method consists in an analysis of the simulation electrical signal (voltage or current) and detect the time it exceeds a predefined limit. The simplest method consists in verifying that the signal does not exceed a margin amplitude, as described in Fig. 8. For example, the figure shows the disturbance of a voltage reference equal nominally to 2.5 V. The following failure criterion is defined: the voltage reference should not vary of more than 20 % of the nominal voltage. Thus the maximum fluctuation is equal to 500 mV. In IC-EMC, the failure criterion is defined as follows: the reference voltage is monitored. The upper and

lower limit of this voltage are defined by clicking on the button  , and filling the fields 'Up Volt with 3 and 2 respectively. If the reference voltage goes beyond the limit 'Up Volt. Limit' or below the limit 'Low Volt. Limit', then a failure is detected and the tool computes the forward power of the disturbance that leads to this failure.

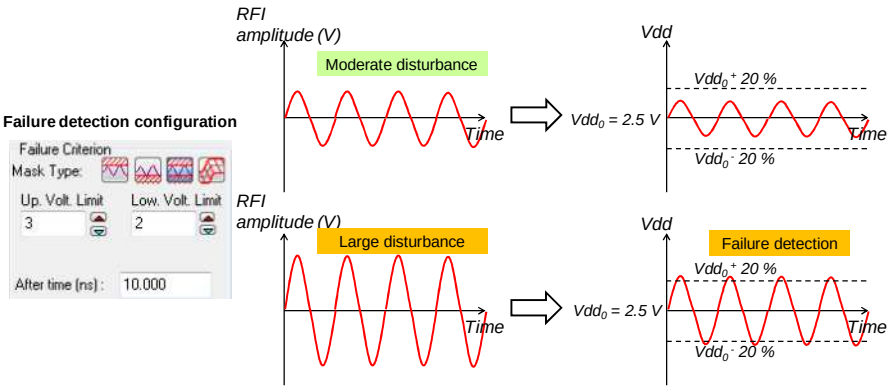


Fig. 8 - Failure criterion definition