Electromagnetic Compatibility of Integrated Circuits (EMC of ICs)

Alexandre Boyer
Alexandre.boyer@insa-toulouse.fr
INSA de Toulouse, France
April 27th, 2009
OUTLINE

AGENDA

9h - 12h: EMC of ICs – part I (Course)
14h - 17h: EMC of ICs – part II (Lab activity)

OBJECTIVES

At the end of the course, the auditor will be able to understand the origins of electromagnetic compatibility (EMC) issues at integrated circuits level, the basic knowledge to face with EMC issues, and become familiar with the most common circuit-level EMC design guidelines.

PRE REQUISITES

Basic knowledge in electrical circuits, CMOS technology, electromagnetism, electrical simulation (SPICE).
Electromagnetic Compatibility of Integrated Circuits (EMC of ICs)

Part I - Course
OUTLINE

CONTENT

- Introduction
- EMC Basics concepts
- Emission/Susceptibility Origin
- Measurement methods
- EMC Guidelines
- Conclusion
1. Introduction
What is EMC?

Two examples

« Disturbances of flight instruments causing trajectory deviations appear when one or several passengers switch on electronic devices. » (Air et Cosmos, April 1993)

29th July 1967: accident of the American aircraft carrier USS Forrestal. The accidental launching of a rocket blew gas tank and weapon stocks, killing 135 persons and causing damages which needed 7 month reparations. Investigations showed that a radar induced on plane wiring a sufficient parasitic voltage to trigger the launching of the rocket.
What is EMC?

« The ability of a device, equipment or system to function satisfactorily in its electromagnetic environment without introducing intolerable electromagnetic disturbance to anything in that environment. »

✓ Reduce parasitic electromagnetic emission and sensitivity or susceptibility to electromagnetic interferences

✓ Guarantee the simultaneous operation of all nearby electric or electronic devices in a given electromagnetic environment

✓ Essential aspect for functional safety of electronic applications
What is EMC?

**EMC certification**

✓ Electronic devices dedicated to critical applications in term of safety and robustness must respond to EMC specifications.

✓ They define maximum levels and methods to characterize emission and susceptibility of an equipment are defined by standards

✓ EMC standards for automotive, aerospace, military, transport, medical, telecommunication applications, but also for commercial products

  - European EMC directive 89/336/EEC about electronic products EMC requirements
  - For automotive applications: ISO 7637, ISO 11452, CISPR 25, SAE J1113
  - For military applications: MIL-STD-461D, MIL-STD-462D
  - For aerospace applications: DO-160
  - For integrated circuits: IEC 61963, IEC 62132

CE mark
Technology trends

Technology (log scale)

- 1μm
- 100nm
- 10nm
- 1nm

Technology trend: cost-performance microcontrollers

Technology trend: high performance microprocessors

Consequences on electronic systems safety, reliability, … and EMC


Technology trends: 0.35μm, 0.25μm, 0.18μm, 0.13μm, 90nm, 65nm, 45nm, 32nm, 22nm, 18nm, 9nm, 7nm

5-years gap
EMC of ICs

Why EMC of ICs

• Until mid 90’s, IC designers had no consideration about EMC problems in their design. EMC was only handled at system and PCB levels.

• Many EMC problems originate from ICs (3rd origin of IC redesign!), as it is the source of noise emission and sensitivity.

• With technology trends (increased clock speed, chip complexity and reduced voltage), ICs are more emissive and sensitive to noise.

• Semiconductor manufacturers are faced with increasing customer expectations for designing low emission and highly immune ICs.

EMC must be handled at IC level.
EMC of ICs

Design issues

EMC problems handled at the end of design cycle

- Design
  - Architectural Design
  - Design Entry
    - Design Architect
- Fabrication
  - Version n°
  - EMC Measurements
    - Compliance?
      - NO GO
      - GO

+ 6 months
+ $$$$$$
EMC of ICs

Design issues

EMC problems handled at the end of design cycle

Architectural Design

Design Entry

Design Guidelines

Tools

Training

EMC Simulations

Compliance?

GO

NO GO

Fabrication

EMC compliant
2. EMC Basic Concepts
## The “EMC” way of thinking

<table>
<thead>
<tr>
<th><strong>Electrical domain</strong></th>
<th><strong>Electromagnetic domain</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage V (Volt)</td>
<td>Electric Field E (V/m)</td>
</tr>
<tr>
<td>Current I (Amp)</td>
<td>Magnetic field H (A/m)</td>
</tr>
<tr>
<td>Impedance Z (Ohm)</td>
<td>Characteristic impedance Z0 (Ohm)</td>
</tr>
<tr>
<td>Z=V/I</td>
<td>Z=E/H</td>
</tr>
<tr>
<td>P=I² x R (watts)</td>
<td>P=H² x 377 (watts/m²)</td>
</tr>
<tr>
<td></td>
<td><em>far field conditions</em></td>
</tr>
</tbody>
</table>
**Specific Units**

### Extensive use of dB for voltage units

Wide dynamic range of signals in EMC → use of dB (decibel)

For example dBV, dBA:

\[
\begin{align*}
\text{dBV} &= 20 \times \log(V) \\
\text{dBA} &= 20 \times \log(A)
\end{align*}
\]

Extensive use of \( dB\mu V \)

\[
V_{dB\mu V} = 20 \times \log \left( \frac{V}{1\mu V} \right) = 20 \times \log(V) + 120
\]

<table>
<thead>
<tr>
<th>Volt</th>
<th>dBV</th>
<th>Milli Volt</th>
<th>dBµV</th>
</tr>
</thead>
<tbody>
<tr>
<td>100</td>
<td>40</td>
<td>1</td>
<td>60</td>
</tr>
<tr>
<td>10</td>
<td>20</td>
<td>0.1</td>
<td>40</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0.01</td>
<td>20</td>
</tr>
<tr>
<td>0.1</td>
<td>-20</td>
<td>0.001</td>
<td>0</td>
</tr>
<tr>
<td>0.01</td>
<td>-40</td>
<td>0.0001</td>
<td>-20</td>
</tr>
<tr>
<td>0.001</td>
<td>-60</td>
<td>0.00001</td>
<td>-40</td>
</tr>
</tbody>
</table>
Specific Units

**Extensive use of dB for power units**

The most common power unit is the “dBm” (dB milli-Watt)

\[ P_{dBmW} = 10 \times \log\left( \frac{P_W}{1mW} \right) = 10 \times \log(P_W) + 30 \]

**Exercise: Specific units**

1 mV = ___ dBµV

0.1 W = ___ dBm

<table>
<thead>
<tr>
<th>Power (Watt)</th>
<th>Power (dBm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 MW</td>
<td>90</td>
</tr>
<tr>
<td>1 KW</td>
<td>60</td>
</tr>
<tr>
<td>1 W</td>
<td>30</td>
</tr>
<tr>
<td>1 mW</td>
<td>0</td>
</tr>
<tr>
<td>1 µW</td>
<td>-30</td>
</tr>
<tr>
<td>1 nW</td>
<td>-60</td>
</tr>
</tbody>
</table>
Specific Units

Emission and susceptibility level units

Conducted emission level (CISPR25)

Radiated emission level (CISPR25)

CISPR 25: “Radio disturbance characteristics for the protection of receivers used on board vehicles, boats, and on devices – Limits and methods of measurement”
Fourier Transform

**Fourier transform: principle**

Time domain measurement

![Oscilloscope](image)

Frequency measurement

![Spectrum analyser](image)

Time

Volt

Freq (Log)

dB

Fourier transform

Invert Fourier transform
Fourier Transform

Why Frequency domain is so important for EMC?

**Time domain**

Only high level harmonics contribution appears

**Frequency domain**

Contribution of each harmonic appears

- Low level harmonics contribution
- User’s specification

FTT
Fourier Transform

Fourier transform - Example

- **50% duty cycle trapezoidal signal**
- **Period** $T = 100$ ns, $Tr = Tf = 2$ ns

FFT

Fast evaluation of signal bandwidth
Two main concepts

Susceptibility to EM waves

- Personal entrainments
- Interferences
- Safety systems
- Printed circuit boards
- Components
- Equipments
- Noise
- System

Emission of EM waves

- Personal entrainments
- Interferences
- Safety systems
- Hardware fault
- Software failure
- Function Loss

Printed circuit boards
Components
Equipment
System
Basic EMC problem

Coupling method:
- Conducted
- Radiated

Solving EMC issues consists in acting on these 3 different elements.
Emission spectrum

Parasitic emission (dBµV)

Emission spectrum

-10 0 10 20 30 40 50 60 70 80

1 10 100 1000

Frequency (MHz)

Sufficient margin

EMC compatible

Specification for an IC emission

Measured emission

Aggressor IC

Radiated emission

Ecole Nationale Superieure des Mines
SAINT-ETIENNE

University

Centrale Marseille
Susceptibility threshold

**Immunity level**

(dBmA)

-40 -30 -20 -10 0 10 20 30 40 50

**Frequency (MHz)**

1 10 100 1000

-40 -30 -20 -10 0 10 20 30 40

Current injection limit

Specification for board immunity

Measured immunity

A very low energy produces a fault

Victim IC
Notion of margin

- To ensure the electromagnetic compatibility, emission or susceptibility levels have to be lower than a nominal target …
- …But it is not sufficient to cancel all risks of failures!
- Margin are required to compensate unpredictable variations and reduce failure appearance probability.

- Margin depends on the safety level required in an application domain:

<table>
<thead>
<tr>
<th>Domain</th>
<th>Lifetime</th>
<th>Margin</th>
</tr>
</thead>
<tbody>
<tr>
<td>Aeronautics</td>
<td>30 years</td>
<td>40 dB</td>
</tr>
<tr>
<td>Automotive</td>
<td>10 years</td>
<td>20 dB</td>
</tr>
<tr>
<td>Consumer</td>
<td>1 year</td>
<td>0 dB</td>
</tr>
</tbody>
</table>
Parasitic coupling mechanisms

Coupling mechanisms

**Conducted mode – Common impedance coupling**

Example: The VSS supply track propagates noise.

**Radiated mode – Antenna coupling**

The EM wave propagates through the air.

- Loop: Magnetic field coupling
- Wire: Electric field coupling
Parasitic coupling mechanisms

**Crosstalk**

- Parasitic coupling between nearby conductors.
- Near field coupling ≠ radiated coupling

**Capacitive crosstalk**

\[ I = C \frac{dV}{dt} \]

**Inductive crosstalk**

\[ V = L \frac{dI}{dt} \]
Impedance

*R, L, C vs. frequency*

**Impedance profile of:**

- 50 ohms resistor
- 100 pF capacitor
- 10 nH inductor
- A real 100 pF SMD capacitor

\[ Z = \text{constant} \]

- \( Z \div 10 \) at each decade
- \( Z \times 10 \) at each decade
Impedance

Passive components – Real model

Ceramic capacitor

Inductor

Carbon resistor

Understand EMC issues requires the knowledge of electronic device parasitics
Interconnections

Interconnect parasitics

- Parasitic resistance
- Parasitic inductance

\[ R = R_{dc} + R_{ac} \]

\[ R_{dc} = \frac{l}{\sigma \pi a^2} \]

\[ R_{ac} = \frac{l}{\sigma 2\pi a \delta} \]

\[ L = \frac{\mu_0 l}{2\pi} \times \left( \ln \left( \frac{2l}{a} \right) - 1 \right) \]

Quasi static approximation: If \( l < \lambda/20 \), interconnections are considered as electrically small.
Interconnections

Characteristic impedance

- From the electromagnetic point of view:

\[ Z_0 = \sqrt{\frac{E}{H}} \]

Link to conductor geometry and material properties

- From the electric point of view:

\[ Z_0 = \sqrt{\frac{R + jL\omega}{G + jC\omega}} \]

lossless conductor

\[ Z_0 \approx \sqrt{\frac{L}{C}} \]

Equivalent electrical schematic
Interconnections

**Impedance matching**

---

**Adapted:** the line is transparent

**Not adapted:** the signal suffers from distortions: ringing, insertion losses

---

Essential for signal integrity and power transfer
Interconnections

Characteristic impedance

What is the optimum characteristic impedance for a coaxial cable?

<table>
<thead>
<tr>
<th></th>
<th>Small conductor</th>
<th>Large conductor</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power handling</td>
<td></td>
<td>x</td>
</tr>
<tr>
<td>Bending</td>
<td>x</td>
<td></td>
</tr>
<tr>
<td>weight</td>
<td>x</td>
<td></td>
</tr>
<tr>
<td>Low loss</td>
<td>x</td>
<td>x</td>
</tr>
<tr>
<td>Small capacitance</td>
<td>x</td>
<td></td>
</tr>
<tr>
<td>Small inductance</td>
<td></td>
<td>x</td>
</tr>
<tr>
<td>Low Impedance</td>
<td>x</td>
<td></td>
</tr>
</tbody>
</table>

**Ideal values:**
- Maximum power: \( Z_0 = 32 \, \Omega \)
- Minimum loss: \( Z_0 = 77 \, \Omega \)

**Cable examples:**
- EMC cable (compromise between power and loss): \( Z_0 = 50 \, \Omega \)
- TV cable (minimize Loss): \( Z_0 = 75 \, \Omega \)
50 Ω adapted equipments

EMC equipments

Spectrum analyzer

Waveform generator

Amplifier

Tem cell

Gtem
3. Origin of Emission and Susceptibility of ICs
Integrated circuits are the origin of parasitic emission and susceptibility to RF disturbances in electronic systems.
Source of Electromagnetic Interferences

- Natural disturbances (cosmic rays, thunder)
- Radio communications, wireless, radars,…
- Electrical Overstress
- Inductive loads, motors
- IC activity

IC
Origin of parasitic emission

Basic mechanisms for CMOS circuit current: CMOS inverter example

- VDD
- Vin
- VSS
- IDD (0.1mA)
- ISS (0.1mA)
- Output capa

Switching current

Voltage

Time

Vout

Main noise sources comes from AC current sources:
- Clock-driven blocks, synchronized logic
- I/O switching
Origin of parasitic emission

- Parasitic emission is linked to voltage drops... But only current peaks cannot explain completely electromagnetic emission.
- Inductance are responsible of the conversion of current peak to voltage drops.
- Current peaks and voltage drops generate the conducted emission and then the radiated emission.

\[ \Delta V = L \frac{\Delta i}{\Delta t} \]
Why technology scale down makes things worse?

- Current level keeps almost constant but:
  - Faster current switching

Stronger di/dt

Increase parasitic noise
Origin of parasitic emission

Example: evaluation of switching current in an IC

- 0.1 mA / Gate in 100ps
- 1 Billion gates (32 Bit Micro) =>
- 10% switching activity =>
- Spreading of current peak (non synchronous switching) =>
Origin of parasitic emission

Example: evaluation of supply voltage bounce

Evaluate noise amplitude:
Origin of parasitic emission

Overview of influent parameters on parasitic emission

1. Internal activity of the IC
2. Output load of the IC
3. Filtering effect of IC interconnections
4. Filtering effect of PCB tracks and external passive devices
Susceptibility issues

Less voltage, more IOs

Supply (V)

Noise margin reduction

Core supply

I/O supply

Supply

0.5µ 0.35µ 0.18µ 90nm 65nm 45nm

0.7 1.2 1.8 2.5 3.3 5.0

100 200 500 1000

Technological

Ecole Nationale Supérieure des Mines
SAINT-ÉTIENNE

Technology

University

Centrale Marseille
Susceptibility issues

Multiple parasitic electromagnetic sources

Components issues

- Radar Météo
- Radars
- Satellites
- TV UHF
- MWave
- Stat. de base
- Badge
- GSM
- UMTS
- DECT
- Radar

Power: 1GW, 1MW, 1KW, 1W, 1mW

Frequency: 3 MHz, 30 MHz, 300 MHz, 3 GHz, 30 GHz, 300 GHz
Susceptibility issues

More complex ICs, more failure types

- Electromagnetic wave
- Software failure
- Hardware fault
- System failure
- Function loss
- µp mixed analog
- More complex ICs, more failure types
**Susceptibility issues**

**Desynchronisation issues**

EMI induced delay is becoming increasingly important in digital design due to rising operating frequencies.
Origin of IC susceptibility

Overview of influent parameters on IC susceptibility

1. Filtering effects of PCB tracks and external passive components
2. Filtering effect of IC interconnections
3. Impedance of IC nodes (high Z node = high susceptibility)
4. Non linear effects of active devices (conversion RF signals to DC offsets !)
5. Block own susceptibility (noise margin, delay margin, …)
## Emission / Susceptibility issues

### Overview of typical emissive/susceptible blocks

<table>
<thead>
<tr>
<th>Block type</th>
<th>Emission</th>
<th>Susceptibility</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. DC/DC converter</td>
<td>+</td>
<td>++</td>
</tr>
<tr>
<td>2. Power switch output</td>
<td>++</td>
<td>--</td>
</tr>
<tr>
<td>3. Charge pump</td>
<td>++</td>
<td>--</td>
</tr>
<tr>
<td>4. Oscillator / PLL / Clock circuitry</td>
<td>++</td>
<td>++</td>
</tr>
<tr>
<td>5. Fast digital I/O</td>
<td>++</td>
<td>-</td>
</tr>
<tr>
<td>6. Digital block supply</td>
<td>+</td>
<td>-</td>
</tr>
<tr>
<td>7. Analog input/supply</td>
<td>--</td>
<td>++</td>
</tr>
<tr>
<td>8. RF front end</td>
<td>+</td>
<td>++</td>
</tr>
</tbody>
</table>
4. EMC measurement methods
EMC measurement methods

Why EMC standard measurement methods

- Check EMC compliance of ICs, equipments and systems
- Comparison of EMC performances between different products, different technologies, designs, PCB routings
- Improve interaction between customers and providers (same protocols, same set-up)
Emission measurement methods

**Emission – General measurement set-up**

- **Device under test**
- **Coupling device**
  - Radiated or conducted coupling
  - Coupling network
  - Antennas
  - Wave guide
- **Control - Acquisition**
  - Acquisition system
  - 50Ω adapted path
- **Verification**
  - Spectrum analyzer
  - EMI receiver
  - Oscilloscope

**Emission requirements verified ?**
# Emission measurement methods

*International standards for IC emission measurement methods*

<table>
<thead>
<tr>
<th>Standard</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>IEC 61967-2</td>
<td>TEM : 1GHz</td>
</tr>
<tr>
<td>IEC 61967-3/6</td>
<td>Near field scan, 5GHz</td>
</tr>
<tr>
<td>IEC 61967-4</td>
<td>1/150 ohm, 1 GHz</td>
</tr>
<tr>
<td>IEC 61967-5</td>
<td>WBFC, 1 GHz</td>
</tr>
<tr>
<td>IEC 61967-7</td>
<td>Mode Stirred Chamber: 18 GHz</td>
</tr>
<tr>
<td>IEC 61967-2</td>
<td>GTEM 18 GHz</td>
</tr>
</tbody>
</table>
Emission measurement methods

GTEM cell: radiated emission up to 18 GHz
Emission measurement methods

IEC 61967-4 International Standard : 1/150 Ohm method

Complex implementation with multiple power pins
Emission measurement methods

IEC 61967-3 International Standard: Near field scan

Microcontroller - 32 MHz scan

Y axis

X axis

dBµV

freq

32MHz

High

Low
Emission measurement methods

IEC 61967-3 International Standard: Silicon scan
Immunity measurement methods

**Immunity – General measurement set-up**

Disturbance generation

- Harmonic signal
- Transients
- Burst

50Ω adapted path

Injected level

Extraction

Coupling device

- Coupling network
- Antennas
- Wave guide

Radiated or conducted coupling

Device under test

Failure detection

**Immunity requirements verified?**
**Immunity measurement methods**

**International standards for IC susceptibility measurement methods**

<table>
<thead>
<tr>
<th>Standard</th>
<th>Description</th>
<th>Image</th>
</tr>
</thead>
<tbody>
<tr>
<td>IEC 62132-2</td>
<td>(Bulk Current Injection : 1 GHz)</td>
<td><img src="image1.png" alt="Image" /></td>
</tr>
<tr>
<td>IEC 62132-3</td>
<td>(Direct Power Inj 1GHz)</td>
<td><img src="image2.png" alt="Image" /></td>
</tr>
<tr>
<td>IEC 62132-4</td>
<td>(TEM/GTEM)</td>
<td><img src="image3.png" alt="Image" /></td>
</tr>
<tr>
<td>IEC 62132-5</td>
<td>(WBFC 1 GHz)</td>
<td><img src="image4.png" alt="Image" /></td>
</tr>
<tr>
<td>New proposal</td>
<td>(LIHA : 10 GHz)</td>
<td><img src="image5.png" alt="Image" /></td>
</tr>
<tr>
<td>Still research</td>
<td>(NFS 10 GHz)</td>
<td><img src="image6.png" alt="Image" /></td>
</tr>
</tbody>
</table>
Immunity measurement methods

IEC 62132-3 International Standard: Direct Power Injection

- **IEC 62132-3**

- **Direct Power Injection**

- **Device under test**

- **Power increase loop until failure**

- **Frequency loop 1 MHz – 3 GHz**

- **10W Amplifier**

- **IEEE Bus**

- **PC Monitoring**

- **Capacitance**

- **Printed Circuit Board**

- **DUT**

- **Good signal**

- **Failure signal**
Immunity measurement methods

IEC 62132-2 International Standard: Bulk Current Injection

- Inductive coupling to the network
- Parasitic current injected on the chip
- Limited to 1 GHz
EMC equipments

- Vector Network Analyzer 10 GHz (100 K€)
- Amplifier 3 GHz 100W (60 K€)
- Spectrum analyzer 40 GHz (40 K€)
- Signal Synthesizer 6 GHz (20 K€)
- GTEM cell 18 GHz (15 K€)

✔ Expensive ....
✔ Complete EMC laboratory : 500 K€
5. EMC guidelines
### Basic concepts to reduce emission and susceptibility

**Remember the influent parameters on emission and susceptibility**

**Emission:**
- Control IC internal activity
- Minimize circuit output load
- Control effect of IC interconnections (decoupling)
- Control effect of PCB interconnections (decoupling)

**Susceptibility:**
- Control effect of PCB interconnections (decoupling)
- Control effect of IC interconnections (decoupling)
- Control Impedance of IC nodes
- Reduce non linear effects of active devices
- Improve block own susceptibility

**Techniques used to reduce emission and/or susceptibility issues are based on these principles**
Golden Rules for Low Emission

Rule 1: Power supply routing strategy

A) Use shortest interconnection to reduce the serial inductance

- Inductance causes voltage bounce
- Each conductor acts as an inductance
- Ground plane modifies inductance value (worst case is far from ground)

Reducing inductance decreases voltage bounce !!

Lead: $L=0.6 \text{nH/mm}$

Bonding: $L=1 \text{nH/mm}$
Golden Rules for Low Emission

Rule 1: Power supply routing strategy

A) Use shortest interconnection to reduce the serial inductance

Leadframe package:
L up to 10nH

Flip chip package:
L up to 3nH

Requirements for high speed microprocessors: L < 50 pH!
Golden Rules for Low Emission

Rule 1: Power supply routing strategy

B) Place enough supply pairs: Use One pair (V_{DD}/V_{SS}) for 10 IOs

Correct

Fail

9 I/O ports
Golden Rules for Low Emission

Rule 1: Power supply routing strategy

C) Place supply pairs close to noisy blocks
Golden Rules for Low Emission

Rule 1: Power supply routing strategy

D) Place VSS and VDD pins as close as possible

- to increase decoupling capacitance that reduces fluctuations
- to reduce current loops that provoke magnetic field
Golden Rules for Low Emission

Rule 1: Power supply routing strategy

Case study 1:

Case 1: Infineon Tricore

Case 2: virtex II
Golden Rules for Low Emission

Rule 1: Power supply routing strategy

Case study 2: 2 FPGA, same power supply, same IO drive, same characteristics. Supply strategy very different!

- More Supply pairs for IOs
- Better distribution

courtesy of Dr. Howard Johnson, "BGA Crosstalk", www.sigcon.com
Golden Rules for Low Emission

Rule 1: Power supply routing strategy

Case 1: low emission due to a large number of supply pairs well distributed

Case 2: higher emission level (5 times higher)

*powered by a range of voltages including 1.5-volt in the near field

(Waveforms time-shifted for visual clarity)

courtesy of Dr. Howard Johnson, "BGA Crosstalk", www.sigcon.com
Golden Rules for Low Emission

Rule 2: Add decoupling capacitor

In order to minimize voltage bounce on power supply and ground reference, impedance between Vdd and Vss must be as low as possible (inferior to a target impedance).

The most efficient method to reach the target impedance is the decoupling capacitor:

- Keep the current flow internal
- Local energy tank
- Reduce power supply voltage drops

\[
Z_t < \frac{V_{dd} \times \text{ripple max}}{\text{current}}
\]

\[
C_{min} = \frac{1}{Z_{max} \times 2\pi \times f_{min}}
\]
Golden Rules for Low Emission

Rule 2: Add decoupling capacitor

Parasitic emission (dBμV)

- Customer’s specification
- 10 – 15 dB

Efficient on one decade

Internal voltage drop
Golden Rules for Low Emission

Rule 2: Add decoupling capacitor

Typical decoupling capacitor placement on power distribution network:

- Electrolytic bulk capacitor: 1 µF – 10 mF
- HF ceramic capacitor: 100 nF – 1 nF
- Ferrite bead
- PCB planes
- On chip interconnections

Voltage regulator

Power supply

Ground
**Golden Rules for Low Emission**

*Rule 2: Add decoupling on-chip capacitor*

- Very high efficient decoupling above 100 MHz (where PCB decoupling capacitors become inefficient) ...
- ... But space consuming
- Fill white space with decap cells
- Use MOS capa. or Metal-Insulator-Metal (MIM) capa.

---

**On chip decoupling capacitance versus technology and complexity**

---

**Capa cell for local decoupling**
Golden Rules for Low Emission

**Rule 3: Reduce core noise**

- Reduce operating supply voltage
- Reduce operating frequency
- Reduce peak current by optimizing activity:
  - using distributed clock buffers
  - turning off unused circuitry
  - avoiding large loads
  - using several operation mode
Golden Rules for Low Emission

Rule 3: Reduce core noise

- Add a controlled jitter on clock signal to spread the noise spectrum

![Diagram showing clock in and clock out with spread spectrum frequency modulation.](image)
Golden Rules for Low Emission

Rule 3: Reduce core noise
- Asynchronous design spreads noise on all spectrum (10 dBµV reduction)
Golden Rules for Low Emission

Rule 4: Reduce I/O noise

- Minimize the number of simultaneous switching lines (bus coding)
- Reduce di/dt of I/O by controlling slew rate and drive
Golden Rules for Low Susceptibility

Rule 1: Add decoupling capacitance

- DPI aggression of a digital core
- Reuse of low emission design rules for susceptibility
- Efficiency of on-chip decoupling combined with resistive supply path

Work done at Eseo France (Ali ALAELDINE)
Golden Rules for Low Susceptibility

Rule 2: Isolate Noisy blocks

Why?
- To reduce the propagation of switching noise inside the chip
- To reduce the disturbance of sensitive blocks by noisy blocks (auto-susceptibility)

How?
- by separate voltage supply
- by substrate isolation
- by increasing separation between sensitive blocks
- By reducing crosstalk and parasitic coupling at package level
Golden Rules for Low Susceptibility

Rule 3: Robustify circuits

Example: Improve noise immunity of IOs

- Add Schmitt trigger on digital input buffer
- Use differential structures for digital IO to reject common mode noise (as Low Voltage Differential Signaling I/Os)
Golden Rules for Low Susceptibility

Rule 3: Robustify circuits

Reduce desynchronisation issues:

- Synchronous design are sensitive to propagation delay variations due to EMI (→ dynamic errors)
- Improve delay margin to reduce desynchronization failures in synchronous design
- Asynchronous logic design is less sensitive to delay compared to synchronous design

Work done at INSA Toulouse/TIMA Grenoble (Fraiddy BOUESSE)
Case study

StarChip #1
Your definitive solution for embedded electronics, 16 bit MPU with 16 MHz external quartz,

- on-chip PLL providing internal 133MHz operating clock.
- 128Kb RAM, 3 general purpose ports (A,B,C, 8bits)
- 4 analog inputs 12 bits, CAN interface

<table>
<thead>
<tr>
<th>SIGNAL</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>Positive supply</td>
</tr>
<tr>
<td>VSS</td>
<td>Logic Ground</td>
</tr>
<tr>
<td>VDD_OSC</td>
<td>Oscillator supply</td>
</tr>
<tr>
<td>VSS_OSC</td>
<td>Oscillator ground</td>
</tr>
<tr>
<td>PA[0..7]</td>
<td>Data port A (programmable drive)</td>
</tr>
<tr>
<td>PB[0..7]</td>
<td>Data port B (programmable drive)</td>
</tr>
<tr>
<td>PC[0..7]</td>
<td>Data port C (programmable drive) external 66MHz data/address</td>
</tr>
<tr>
<td>ADC In [0..3]</td>
<td>4 analog inputs (12 bit resolution)</td>
</tr>
<tr>
<td>CAN Tx</td>
<td>CAN interface (high power, 1MHz)</td>
</tr>
<tr>
<td>CAN Rx</td>
<td>CAN interface (high power, 1MHz)</td>
</tr>
<tr>
<td>XTL_1, XTL_2</td>
<td>Quartz oscillator 16MHz</td>
</tr>
<tr>
<td>CAPA</td>
<td>PLL external capacitance</td>
</tr>
<tr>
<td>RESET</td>
<td>Reset microcontroller</td>
</tr>
</tbody>
</table>
StarChip #1
Initial floorplan
Case study

StarChip #1
Your floorplan
6. Conclusion
Conclusion

✓ With technology scale down, ICs become more sensitive and emissive.
✓ EMC of ICs has become a major concerns for ICs suppliers
✓ Basic concepts are necessary to make preliminary analysis of EMC problems and propose first solutions
✓ Origins of emission and susceptibility issues at IC level have been described. Their knowledge is required to apply EMC design guidelines.
✓ The classical EMC design guidelines at IC level have been presented: reducing inductances, adding decoupling capacitor, reducing core activity, robustify circuits, isolating noise blocks from sensitive blocks).
Electromagnetic Compatibility of Integrated Circuits (EMC of ICs)

Part II – Lab Activity
IC-EMC software

✓ Illustrate EMC of ICs notions through different problems.
✓ Solving these problems with the assistance of the software IC-EMC.

IC-EMC is a friendly and free PC tool developed at INSA de Toulouse for modeling and simulating EMC at IC level. The tool is linked with the freeware WinSPICE derived from SPICE Berkeley for analog simulation.

Download IC-EMC and WinSPICE at:

http://www.ic-emc.org

Version used in 2009: version 2.0 “beta”
IC-EMC main screen

IC-EMC simulation tools

Simulation command

Symbol palette

Schematic capture interface
Simulation flow with IC-EMC

IC-EMC schematic Editor (.sch)  
IC-EMC model libraries

WinSPICE compatible netlist generation (.cir)

WinSPICE simulation

IC-EMC Post-processing tools (emission, impedance, S-parameters, immunity)

Measurement result files import

Output file generation
### Most important icons

<table>
<thead>
<tr>
<th>Icon</th>
<th>Description</th>
<th>Icon</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>![Folder]</td>
<td>Open schematic (.sch)</td>
<td>![Green Button]</td>
<td>Build SPICE netlist (.cir)</td>
</tr>
<tr>
<td>![Folder]</td>
<td>Save schematic (.sch)</td>
<td>![Blue Waveform]</td>
<td>Spectrum analysis</td>
</tr>
<tr>
<td>![Copy]</td>
<td>Copy symbols</td>
<td>![Copy]</td>
<td>Immunity simulation</td>
</tr>
<tr>
<td>![Arrow]</td>
<td>Move symbols</td>
<td>![Arrow]</td>
<td>Time domain analysis</td>
</tr>
<tr>
<td>![Rotate]</td>
<td>Rotate symbols</td>
<td>![Rotate]</td>
<td>Impedance simulation</td>
</tr>
<tr>
<td>![Flip]</td>
<td>Flip symbols</td>
<td>![Flip]</td>
<td>S parameter simulation</td>
</tr>
<tr>
<td>![Add Text]</td>
<td>Add Text line</td>
<td>![Ibis]</td>
<td>Ibis file editor</td>
</tr>
<tr>
<td>![Add Line]</td>
<td>Add a line</td>
<td>![Symbol Palette]</td>
<td>Symbol palette</td>
</tr>
<tr>
<td>![View]</td>
<td>View electrical net</td>
<td>![View]</td>
<td>View all schematic</td>
</tr>
</tbody>
</table>
SPICE simulation

✓ WinSPICE interface:
✓ Click File/Open to open a circuit netlist (.cir) generated by ic-emc.
✓ When the netlist is opened, each time the netlist is regenerated, a simulation is launched again.
✓ Main simulation commands for IC-EMC:

<table>
<thead>
<tr>
<th>Simulation command</th>
<th>Command line</th>
<th>Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transient simulation</td>
<td>.tran 0.1n 100n</td>
<td>step + stop time</td>
</tr>
<tr>
<td>DC simulation</td>
<td>.DC Vdd 0 5 0.1</td>
<td>source + start + stop + step</td>
</tr>
<tr>
<td>Small signal freq. analysis</td>
<td>.AC LIN/DEC 100 1MEG 1G</td>
<td>sampling + nb points + start + stop</td>
</tr>
<tr>
<td>Load SPICE library</td>
<td>.lib spice_lib.lib</td>
<td>Path and file name</td>
</tr>
</tbody>
</table>
Problem 1 – Crosstalk evaluation

Two nearby microstrip lines are drawn on a 1.6 mm thick FR4 printed circuit board ($\varepsilon_r = 4.5$). The lines are 0.5 mm wide, 35 µm thick and 1 cm long, and separated by a 0.25 mm gap. One line is supplied by a voltage generator and is called the aggressor line, while the second is not supplied and is called the victim line. This exercise aimed at computing the maximum amplitude of the noise coupled on the victim line due to crosstalk.

1. Compute the electrical parameters of these lines. (Use Tools/Interconnect parameters)

2. A square signal supplied one of the line. Its characteristics are:
   - $V_{\text{min}} = 0$ V, $V_{\text{max}} = 5$ V
   - Period = 100 ns, duty cycle = 50 %
   - Rising and fall time = 2 ns
   - Output impedance $R_s1 = 50$ Ω

Is the quasi static approximation satisfied over all the bandwidth of the signal?
Problem 1 – Crosstalk evaluation

3. The 3 other input/output ports of these 2 lines are loaded by 50 $\Omega$ resistors. VFE and VNE are the far end and near end voltage. Propose an equivalent electrical schematic of these coupled lines.

4. Propose an equivalent model for the victim line. Deduce literal expressions of far end and near end peak voltage on the victim line.

5. Verify your expression in simulation.

6. Could this parasitic coupling involve EMC problems?

7. Is the literal expressions are still valid for a 10 cm line?
Problem 2 – Simultaneous switching noise

Let’s consider the case of the following single output buffer. It is modelled as a CMOS inverter with the given dimensions. Models of MOS transistors are included in the file lib_SPICE.lib. This buffer is driven by a predriver stage that we model as a square generator with the following characteristics:

- $V_0 = 0 \, \text{V}, \, V_1 = 5 \, \text{V}$
- $T_r = T_f = 1 \, \text{ns}$
- Period = 100 ns
- $P_W = \text{Period} - T_r$ (to keep a 50 % duty cycle)

The output buffer will be loaded with a capacitance. The conducted noise on supply lines will be probed with a 1 $\Omega$ resistor placed on $V_{ss}$ path of the buffer.

1. Build the schematic of the I/O loaded by 10 pF. Observe the transient response across the 1 $\Omega$ probe. Comment. Deduce the amplitude of dynamic consumption of current.
2. Load the output of the buffer with different values of capacitance (from 10 fF to 1 nF). Observe the transient response of voltage across the 1 Ω probe and comment.

3. Load the output with a 47 pF capacitor. Plot the FFT of the voltage across Vss. What is the bandwidth of the noise?

4. Do the simulation of question 3 for Tr = 5 ns. Comment the result.

5. The load is connected to the buffer through a 4 cm long, 0.5 mm wide tracks drawn on a 1.6 mm FR4 PCB. Inductance of the package is estimated about 6 nH. Observe the transient response and the spectrum of voltage across the 1 Ω probe and comment.

6. Inductance on power supply and ground reference are estimated at 10 nH (PCB planes and package). Does it influence the power integrity?

7. Simulate the noise on ground reference for a 8 I/O port. Propose a solution to reduce the noise amplitude.
To predict parasitic emission of digital core of integrated circuits, macromodelling as ICEM model (IEC 62433) is often used to provide accurate results with a low complexity model. It simplifies the activity of a digital core to one or several equivalent current sources and the complex power distribution network to a passive network composed of several R, L, C elements.

IC-EMC provides a tool called ICEM model expert (Tools/ICEM model expert) which helps generating ICEM model of a digital circuit based on basic information.

Let’s consider the following 16 bit microcontroller:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>0.12 µm</td>
</tr>
<tr>
<td>Core supply voltage</td>
<td>1.2 V</td>
</tr>
<tr>
<td>Bus clock frequency</td>
<td>20 MHz</td>
</tr>
<tr>
<td>Number of gates</td>
<td>100 K</td>
</tr>
<tr>
<td>Gate activity</td>
<td>15 %</td>
</tr>
<tr>
<td>IC size</td>
<td>15 mm²</td>
</tr>
<tr>
<td>Package</td>
<td>QFP</td>
</tr>
<tr>
<td>number of core supply pairs</td>
<td>1</td>
</tr>
<tr>
<td>Performance</td>
<td>Standard</td>
</tr>
<tr>
<td>Emission measurement</td>
<td>0.1 ohm</td>
</tr>
</tbody>
</table>

1. Use the tool ICEM model expert to generate the ICEM model of this microcontroller. Simulate the voltage noise measured across the 0.1 Ω probe. What information does this voltage provide?
Problem 3 – Digital core conducted emission

2. Simulate the IC internal power supply and ground voltage. Is the voltage references are acceptable for a safe operation?

3. The constraint in term of maximum emission level from 150 KHz to 1 GHz is defined as ‘H8’ (definition from standard IEC71967). What is the effect of 2 additional supply pairs on conducted noise? On internal noise?

4. A “traditional” 100 nF ceramic capacitor external capacitor is added. Its real model includes a serial 0.5 nH inductor and a 100 mΩ resistor. Effect of PCB is neglected. Trace its impedance profile between 1 MHz and 1 GHz. On which frequency band this capacitor decouples efficiently? What is its effect on the conducted emission? On the internal noise?

5. Add further external decoupling capacitances (keep the same values for R and L values for capacitance parasitics). Adjust their numbers and their values to ensure the specification in term of emission.

6. Adjust the internal activity to reduce the emission level enough to satisfy the maximum emission criterion.
Problem 4 – Decoupling and conducted emission

The circuit describes in problem 3 is mounted on a 2 layers PCB. The following schematic describes the top layer of the PCB, where the components are mounted. The bottom side is a full ground plane. Characteristics of the PCB is: FR4 (\(\varepsilon_r = 4.6\), height = 1.6 mm).

All the components are surface mounted devices. The schematic describes the connection of Vdd and Vss pins of the circuit to the power supply and ground references assured by a regulator. These references are supposed ideal. A 0.1 \(\Omega\) resistor is added across the Vss pin.

1. Build the equivalent model of the circuit (use Tools/ICEM model expert) and the PCB (use Tools/Interconnect parameters). Simulate the voltage measured across the 0.1 \(\Omega\) probe. What information does this voltage provide?
Problem 4 – Decoupling and conducted emission

2. The constraint in term of maximum emission level from 150 KHz to 1 GHz is defined as ‘H8’ (definition from standard IEC71967). Does the circuit check the conducted emission requirements?

3. 1 ceramic 100 nF capacitor is a typically used as decoupling capacitor for digital circuits. Place a 100 nF capacitor close to the circuit. What is the effect on the conducted noise?

4. Is the previous model realistic? Add a more realistic model of capacitor. Test the placement of the capacitor.

5. Simulate the impedance seen from the pins Vdd/Vss of the circuit with and without the 100 nF decoupling capacitor. What is the link with the conducted emission?

6. Add several decoupling capacitor to make the circuit compliant to the conducted emission requirements.
Problem 5 – Conducted susceptibility of a digital circuit

In this problem, the circuit described in problem 3 is reused. A digital I/O is supplied by the power supply. Model of this I/O is described in problem 2. The I/O is loaded by a 47 pF. The circuit is mounted on a PCB, described in problem 4.

To test the conducted susceptibility of this circuit to RF disturbances, the Direct Power Injection (DPI) method is used. The RF disturbance is coupled to a low frequency signal by a bias tee. As susceptibility threshold is given in term of forward power, a directional coupler is used to extract this value. Delay of this coupler is 2 ns.

The susceptibility criterion is given in term of the noise on the output voltage of the I/O. It must remain inferior to 20% of the power supply voltage.

1. The bias tee should have the following properties: transmission between RF input and output > -3 dB, RF input reflected coefficient > -10 dB. Tune the passive elements of the bias tee to check these properties from 1 MHz to 1 GHz. Use S parameter simulation.
Problem 5 – Conducted susceptibility of a digital circuit

2. Connect the bias tee and the RF injection system to a 100 Ω load. Simulate the susceptibility threshold for a maximum noise of 1 V across the load. Would it be possible to predict the susceptibility threshold without SPICE simulation?

3. Build the equivalent model of the circuit (use Tools/ICEM model expert) and the PCB (use Tools/Interconnect parameters, remove the 1 Ω probe). Simulate the susceptibility threshold of circuit.

4. Simulate the reflection coefficient of the circuit. Does a link exist between the susceptibility threshold and the reflection coefficient?

5. If a decoupling capacitor is added between Vdd and Vss, what will be the effect on circuit susceptibility? Verify your conclusion by simulation.