INSA INSTITUT NATIONAL DES SCIENCES APPLIQUÉES TOULOUSE

# Analog and RF CMOS circuit design

# Design of a fully integrated wireless power transmitter– Some theoretical elements

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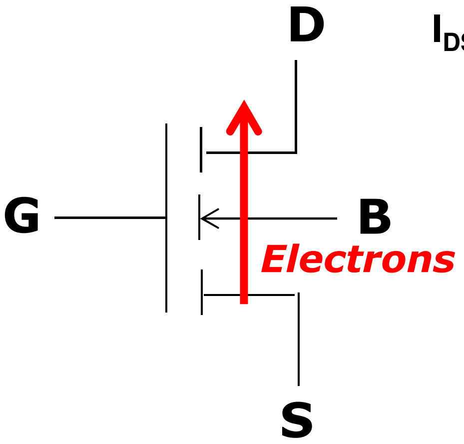
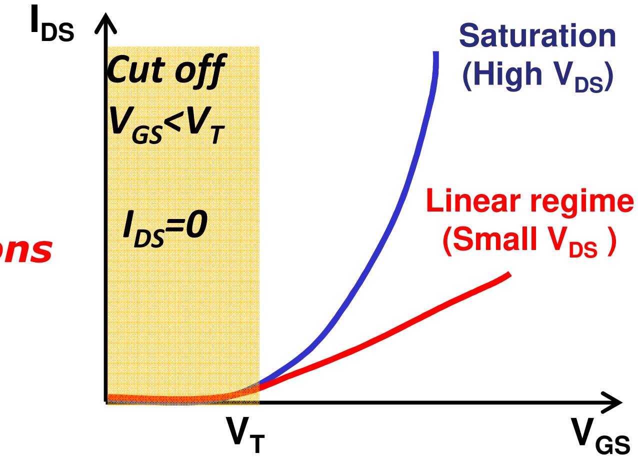
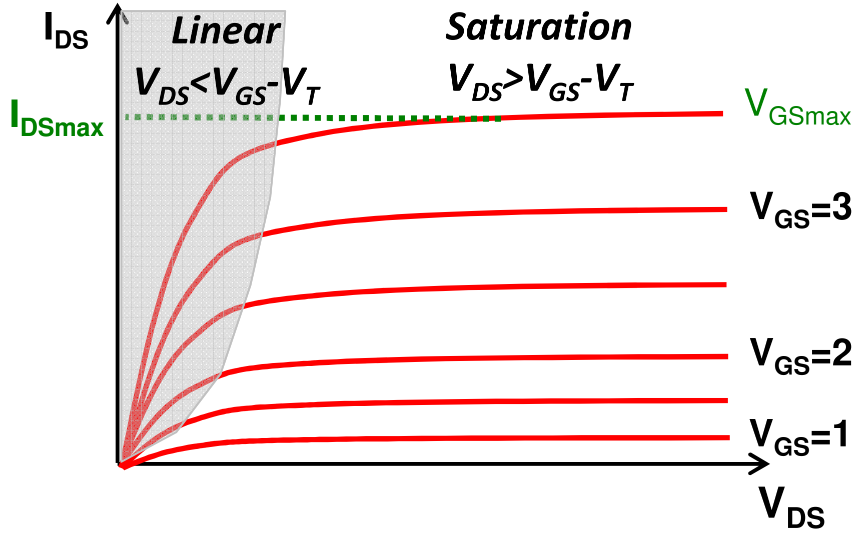
# Simplified operation of MOSFET

NMOSFET




Static operating point (simplified model for long channel only)

**Linear regime** ($V_{DS} < V_{GS}$-$V_T$) **:**

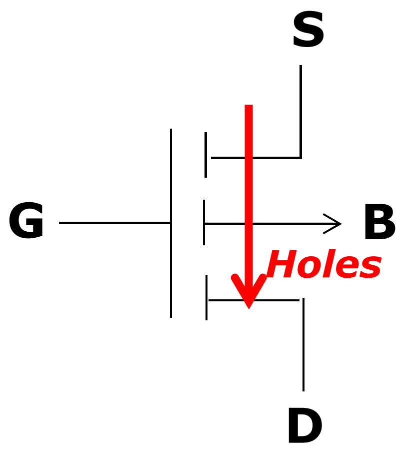
$$\mathrm{Ids} = K((\mathrm{V_{gs}} - \mathrm{V_T}).\mathrm{V_{ds}} - \frac{(\mathrm{V_{ds}})^2}{2})) \times (1 + \lambda \mathrm{V_{ds}})$$

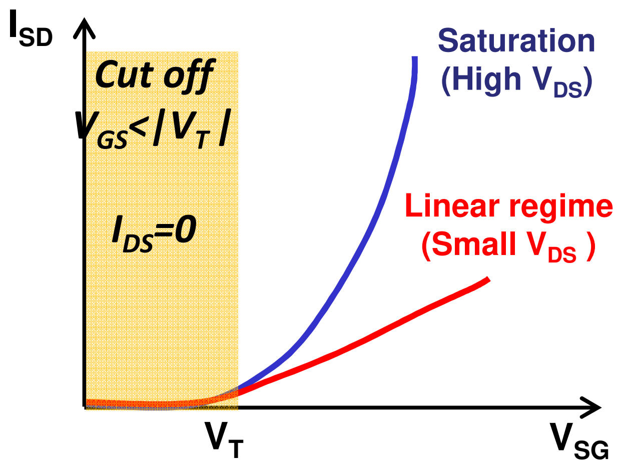
**Saturation** ($V_{DS} > V_{GS}$-$V_T$) **:**

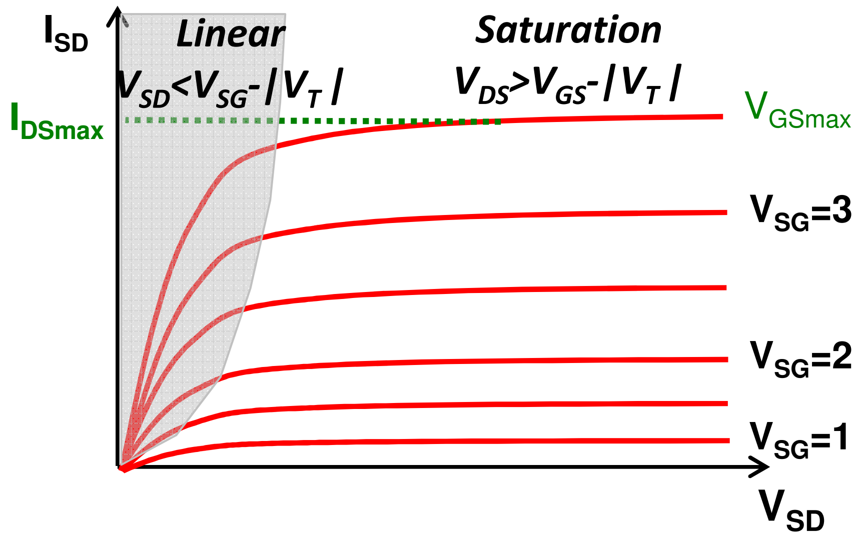
$$\mathrm{Ids} = \frac{1}{2} K (V_{GS} - V_T)^2 \times (1 + \lambda V_{ds})$$

- In saturation , $I_{DS}$ depends only on $V_{GS}$
- Relationship between $I_{DS}$ and $V_{GS}$ is non-linear
- Equivalent to a voltage-controlled current source

PMOSFET



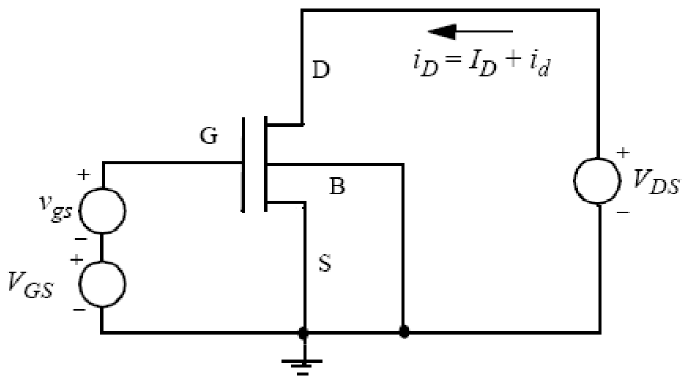

Static operating point (simplified model for long channel only)

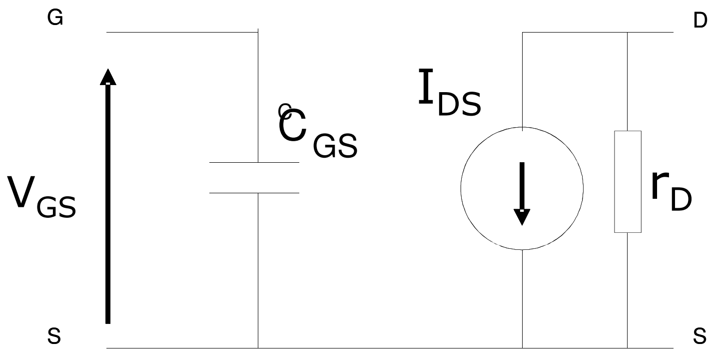
**Linear regime** ($V_{SD} < V_{SG} - |V_T|$) : $\mathrm{Isd} = K((\mathrm{V_{sg}} - |\mathrm{V_T}|).\mathrm{V_{sd}} - \frac{(\mathrm{V_{sd}})^2}{2}))\times(1+\lambda \mathrm{V_{sd}})$

**Saturation** ($V_{SD} > V_{SG} - |V_T|$ ) : $\mathrm{Isd} = \frac{1}{2}K\left(V_{SG} - |V_T|\right)^2 \times (1+\lambda V_{sd})$

- In saturation , $I_{DS}$ depends only on $V_{GS}$
- Relationship between $I_{DS}$ and $V_{GS}$ is non-linear
- Equivalent to a voltage-controlled current source

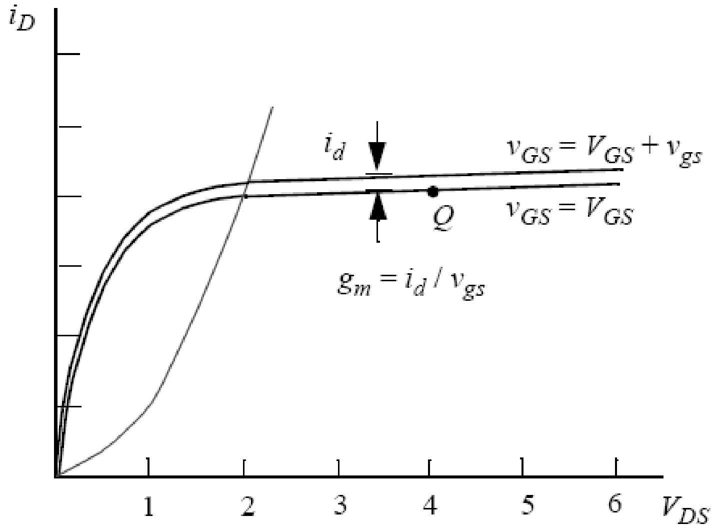
## In saturation regime ($V_{DS} > V_{GS}-V_T$) :




$$C_{gs} \approx \frac{2}{3}(WLC_{ox})$$

$$I_{ds} = g_m V_{gs}$$




$$g_m \equiv \frac{\partial I_{DS}}{\partial V_{GS}} = K(V_{GS} - V_{Th})$$

**Fit by designer**

$$g_m = UO \frac{\varepsilon_0 \varepsilon_r}{TOX} \cdot \boxed{\frac{W}{L}} (V_{GS} - V_{Th})$$

The transconductance sets the voltage, current or power gain of amplifier stage

- Technology CMOS 0.35 µm 50 V (process H35B4S1)
- Integration on the same chip of power drivers (50 V) with command command and analog processing (3.3/5 V)
- Old technological node, but reliable, robust and low-cost technology → adapted to automtive industry
- Available devices (refer ENG-238_rev6.pdf) :
    - NMOS/PMOSFET (LV and HV cores - 3.3 V à 50 V)
    - BJT vertical and lateral NPN/PNP
    - Diodes
    - Resistor (diffusion, Nwell, POLY1/2/H)
    - Cpacitor (MIM, POLY, POLY-Metal)

- MOSFET
  - List of available NMOSFET

| MOSFET | HV CMOS core | 5V gate | 20V gate | NMOS50 | Substrate logic | Isolated low VT |
|---|---|---|---|---|---|---|
| NMOS | x | | | x | x | |
| NMOS20H | x | | x | | | |
| NMOS20HS | x | | x | | | |
| NMOS20M | x | x | | | | |
| NMOS20T | x | | | | | |
| NMOS50H | x | | x | x | | |
| NMOS50HS | x | | x | x | | |
| NMOS50M | x | x | | x | | |
| NMOS50T | x | | | x | | |
| NMOSDI20H | x | | x | | | |
| NMOSDI20M | x | x | | | | |
| NMOSDI50H | x | | x | | | |
| NMOSH | x | | | x | x | |
| NMOSI | x | | | | | |
| NMOSI20H | x | | x | | | |
| NMOSI20M | x | x | | | | |
| NMOSI20T | x | | | | | |
| NMOSI50H | x | | x | | | |
| NMOSI50M | x | x | | | | |
| NMOSI50T | x | | | | | |
| NMOSIL | x | | | | | x |
| NMOSIM | x | x | | | | |
| NMOSIML | x | x | | | | x |
| NMOSM | x | x | | x | x | |
| NMOSMH | x | x | | x | x | |

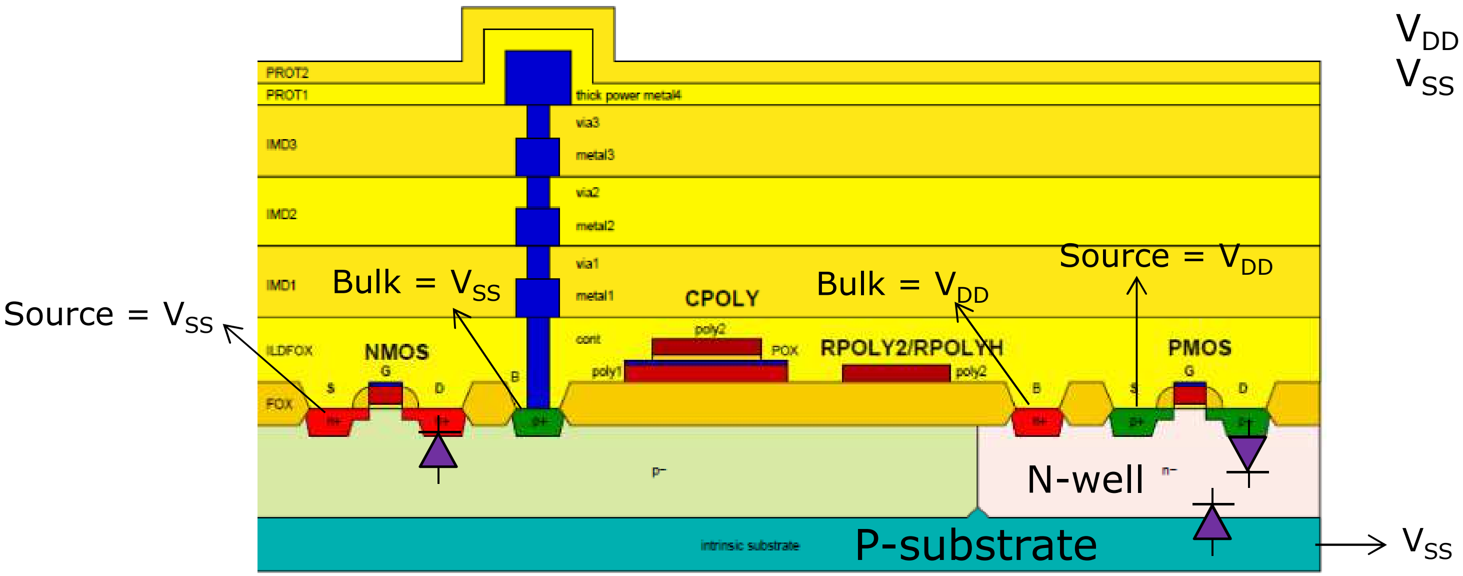
✓ Nominal voltage: 3.3 V, 5 V, 20 V, 50 V (Vgs, Vds, Vdb)

✓ Isolated and non-isolated version

- MOSFET – Wafer cross-section (ENG-236_rev6.pdf)

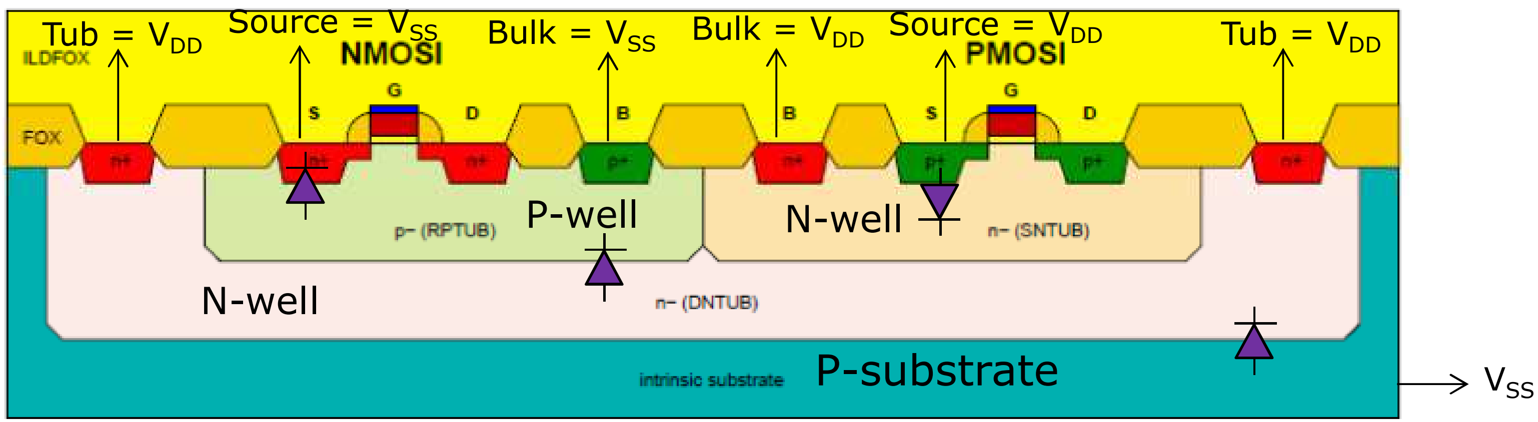
$V_{DD}$ = 3.3 – 5 V
$V_{SS}$ = 0 V

Standard 3.3V / 5V Process



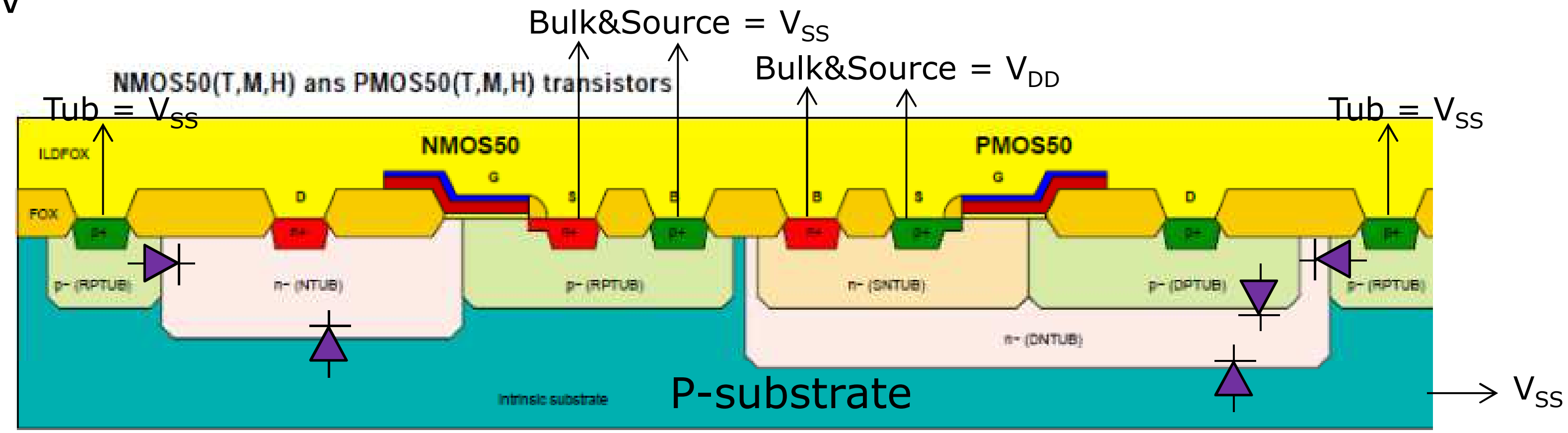

Isolated low voltage (3.3V and 5 V) NMOSI and PMOSI transistors

Junction-based isolation

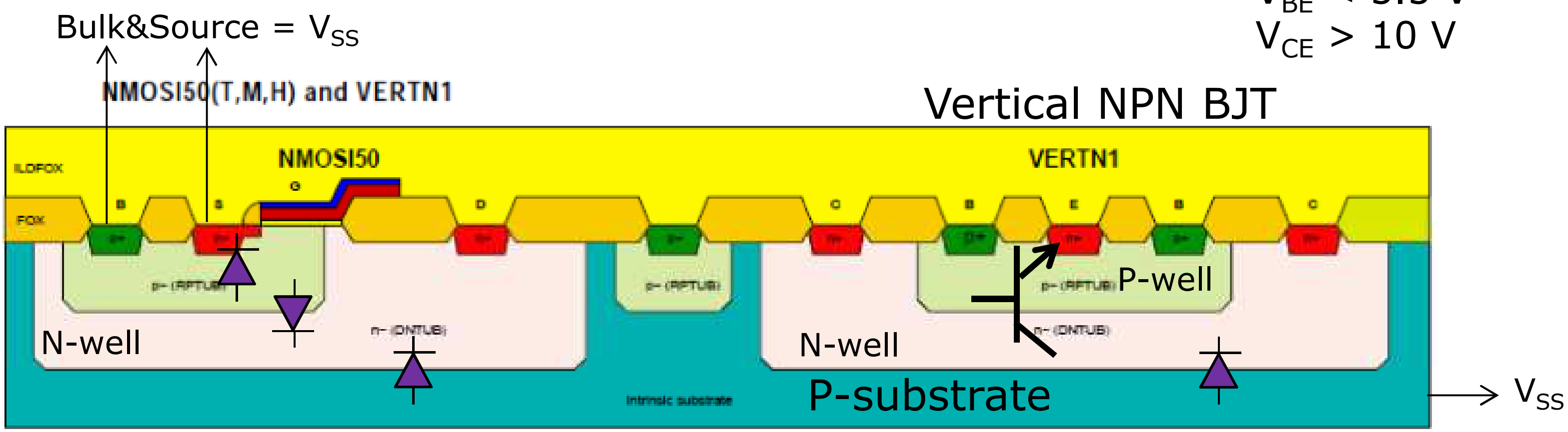


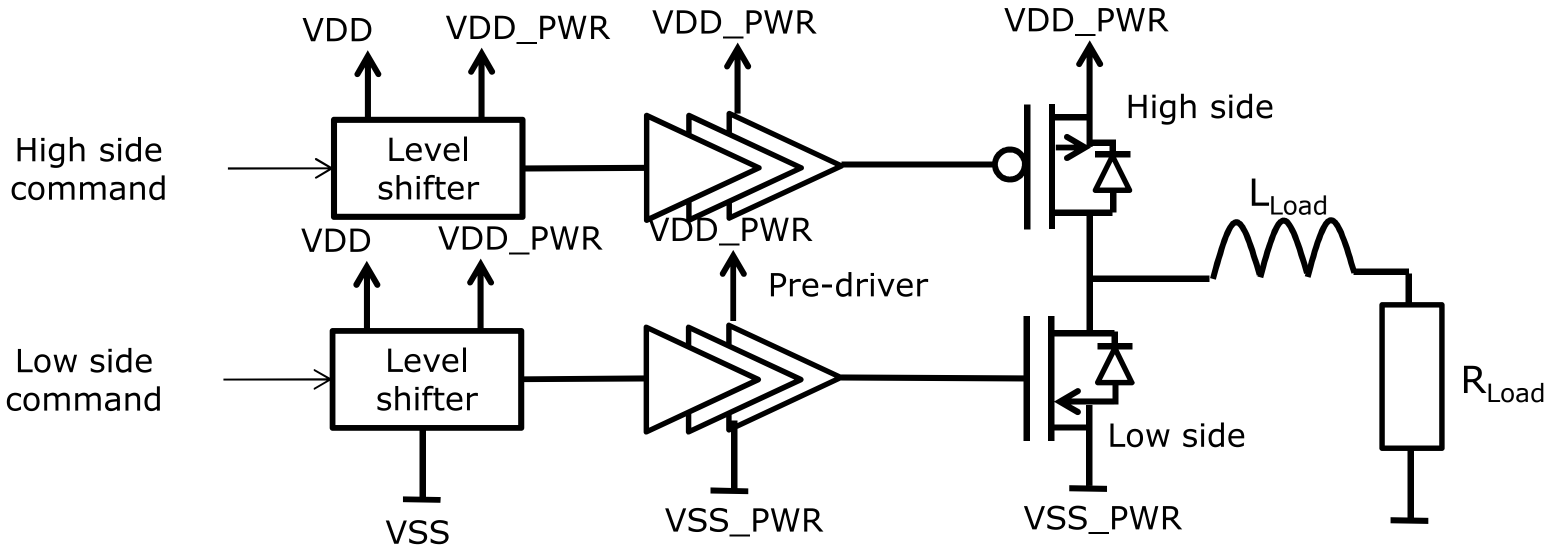
- MOSFET – Wafer cross-section (ENG-236_rev6.pdf)

$V_{DD} < 50$ V
$V_{SS} = 0$ V




$V_{BE} < 5.5$ V
$V_{CE} > 10$ V





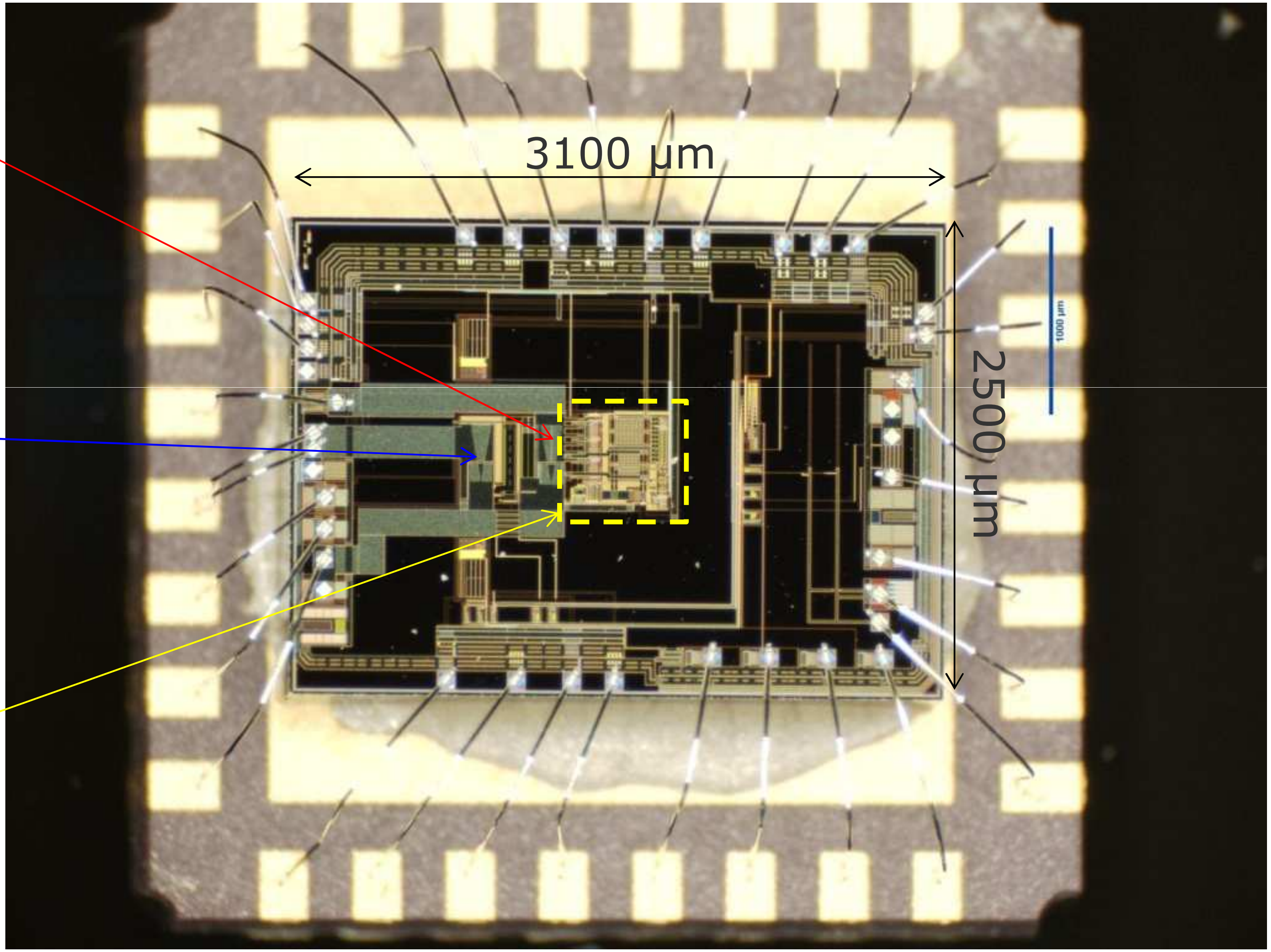

- Constraints :
  - Efficiency optimization (reduce power losses)
  - Small Ron → small drain-source voltage drop → reduction of power dissipation
  - Dead time (remove « crossbar current » or « shoot-through current »)
  - Robustness to overvoltage
  - Slew rate control (EMC)

- Smart Power IC example (High Voltage CMOS 0.35 µm) – Imax = 1 A

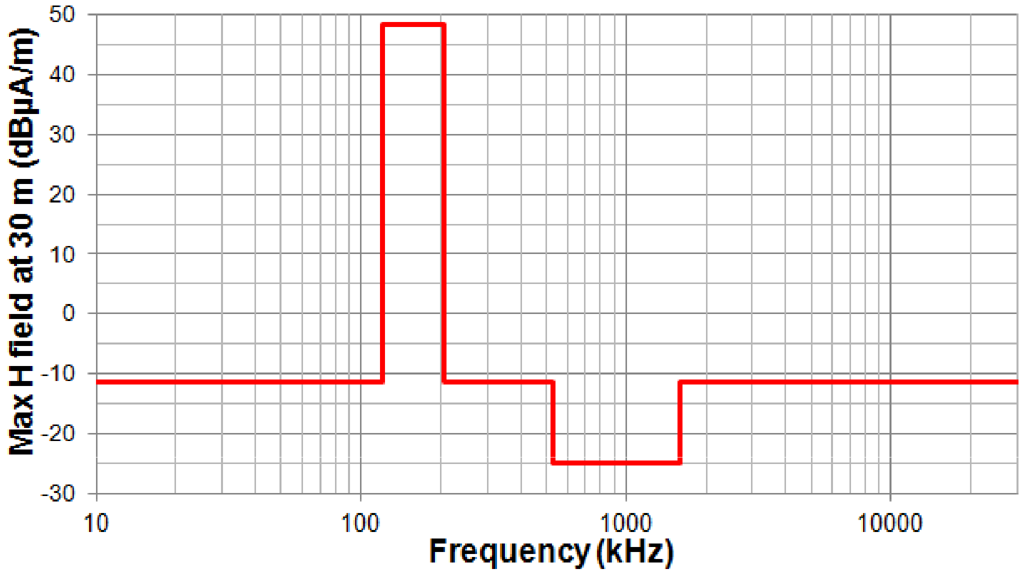
High side
(W=9500 µm,
L= 0.7 µm

Low side
(W=7000 µm,
L= 0.7 µm

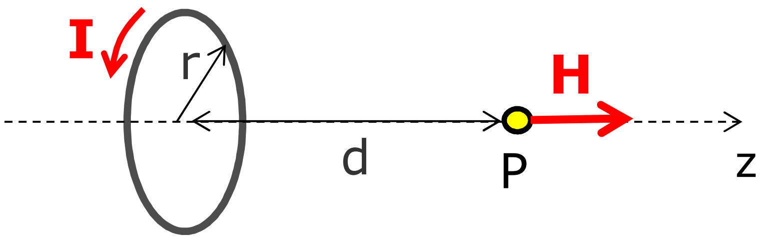
Command +
pre-driver +
on-chip
diagnosis



- EMC constraints: maximum magnetic field H emission (EN55011)

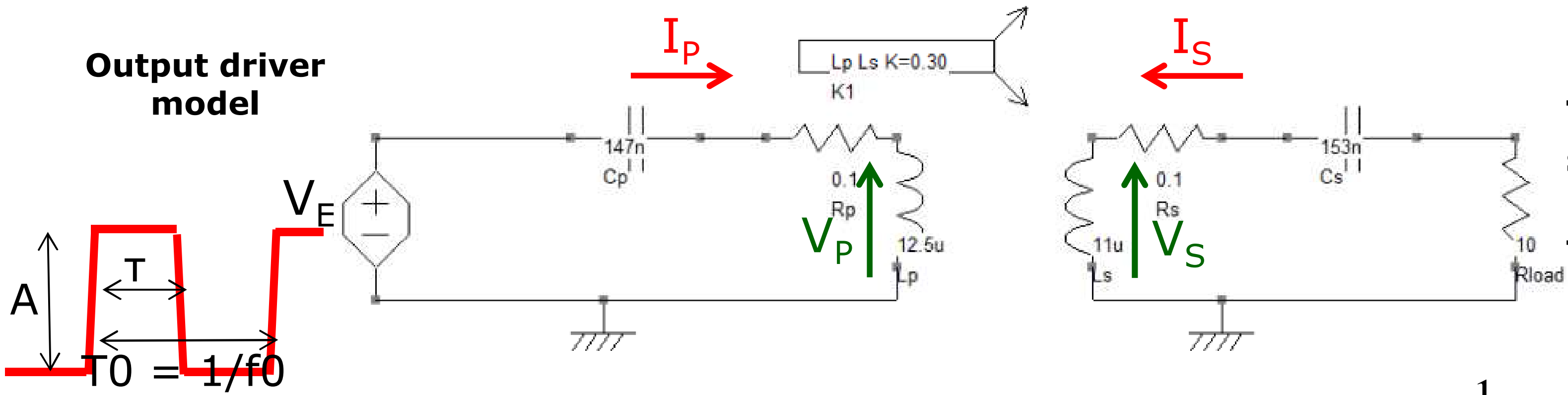



- Magnetic field emission model derived from a N turn small circular loop excited by a constant current




$$H\,(A/m) = \frac{Nr^2 I}{2\left(r^2 + d^2\right)^{3/2}}$$

- Equivalent electrical model:




**The loads is supposed resistive and fixed**

- Inductive coupling coefficient: $k = \dfrac{M}{\sqrt{L_P L_S}}$ $\qquad f_{res} = \dfrac{1}{2\pi\sqrt{L_P C_P}} = \dfrac{1}{2\pi\sqrt{L_S C_S}}$
- Harmonic analysis:

$$\begin{cases} v_{Lp} = jL_P\omega i_p + jM\omega i_s \\ v_{Ls} = jL_S\omega i_S + jM\omega i_P \end{cases} \Rightarrow \quad I_S = \frac{-jM\omega}{M^2\omega^2 + Z_P Z_S} V_E \qquad I_P = \left(1 - \frac{M^2\omega^2}{M^2\omega^2 + Z_P Z_S}\right)\frac{V_E}{Z_P}$$

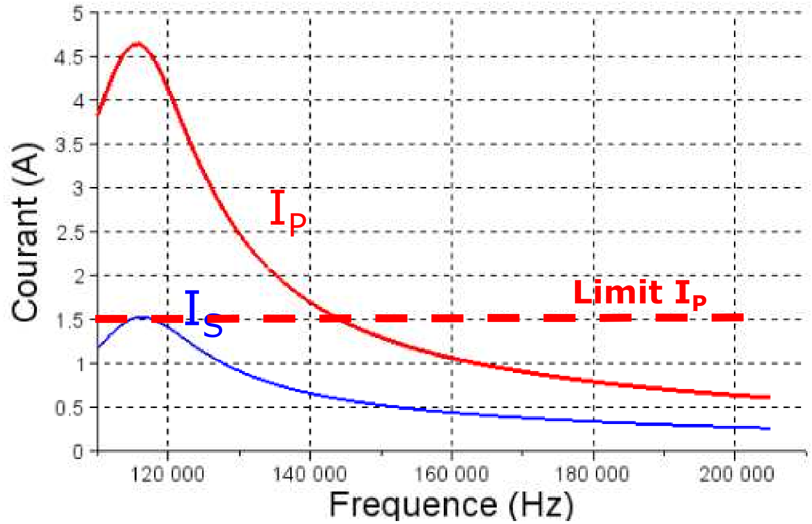
Avec : $Z_P = R_P + jL_P\omega + \dfrac{1}{jC_P\omega}$ $\qquad Z_S = R_{Load} + R_S + jL_S\omega + \dfrac{1}{jC_S\omega}$

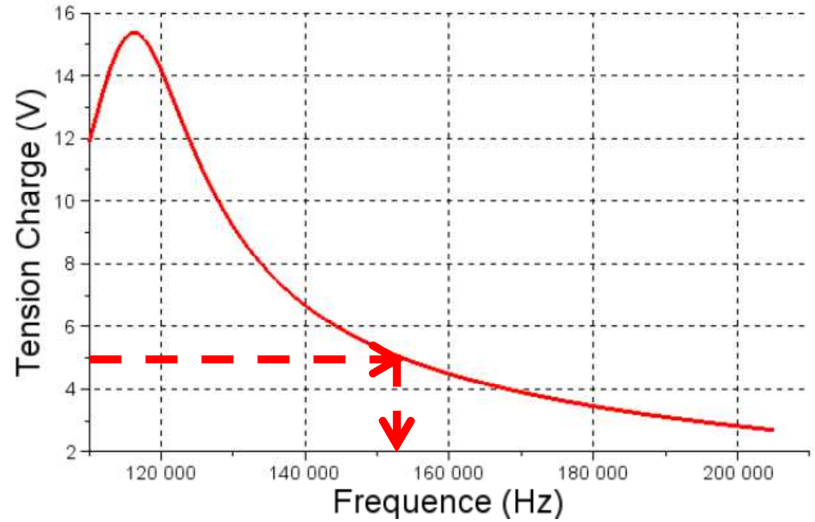
- First harmonic assumption:

Square signal command $\quad \left|V_E(nf_0)\right| = \dfrac{2A\tau}{T_0}\left|\dfrac{\sin\left(\dfrac{n\pi\tau}{T_0}\right)}{\dfrac{n\pi\tau}{T_0}}\right| \Rightarrow \left|V_E(f_0)\right| = \dfrac{2A}{\pi} \quad si\ \tau = \dfrac{T_0}{2}$

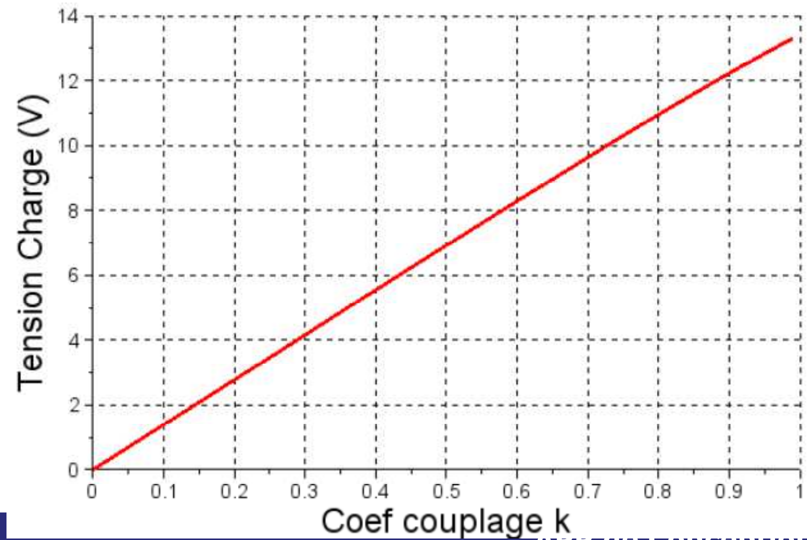
- Example :

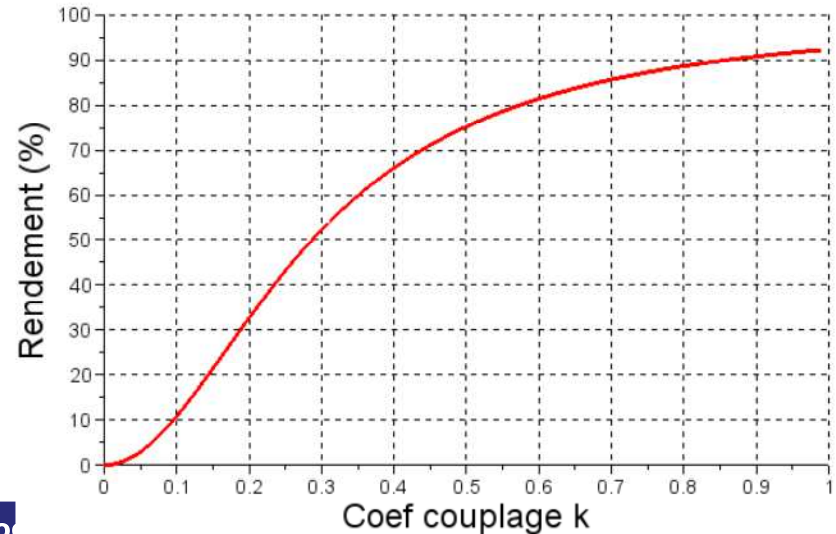
$F_{res}$ = 117 kHz, $\tau = T_0/2$, A = 9 V, k = 0.4, $R_L$ = 10 Ω



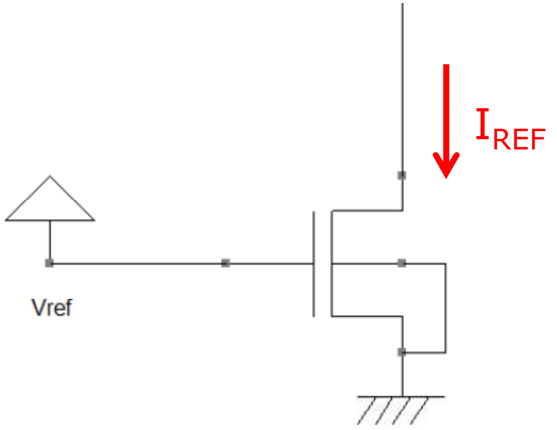

$F_{res}$ = 117 kHz, $F_0$ = 150 kHz, $\tau = T_0/2$, A = 9 V , $R_L$ = 10 Ω



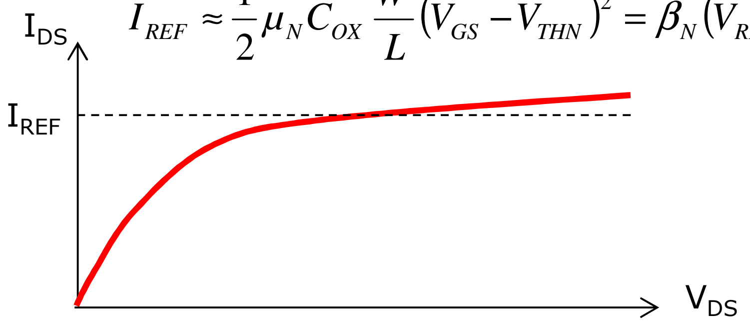



- Some elementary analog structures

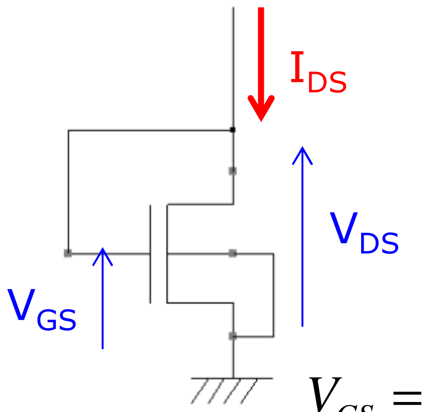
Current source (basically, a NMOSFET or PMOSFET in saturation)




$$I_{REF} \approx \frac{1}{2}\mu_N C_{OX}\frac{W}{L}(V_{GS}-V_{THN})^2 = \beta_N(V_{REF}-V_{THN})^2$$

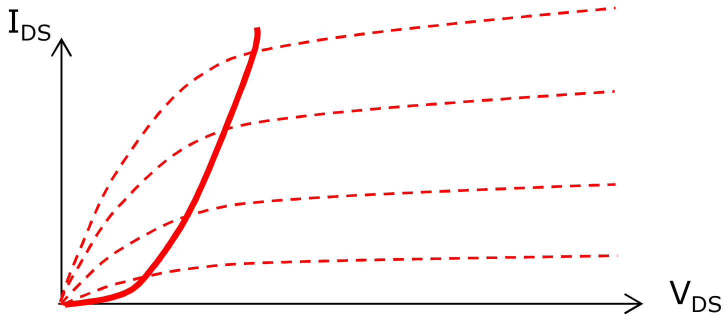



MOSFET-based diode (Active load → compact load)



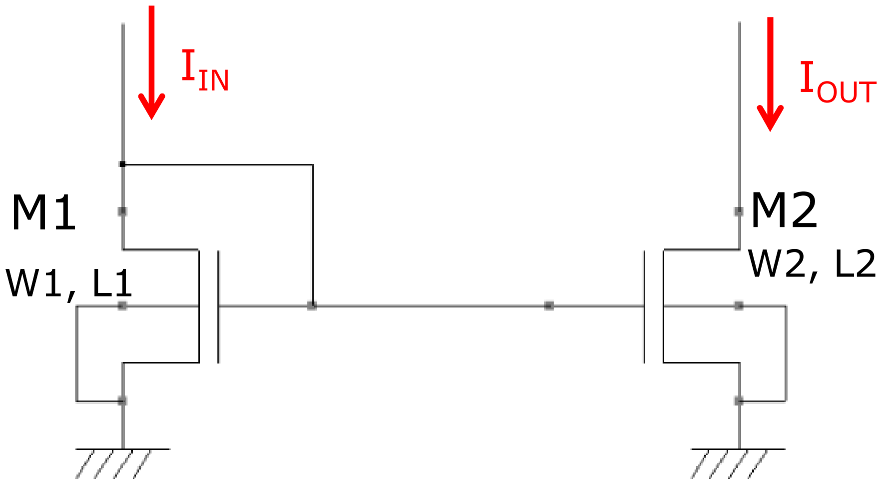

$$V_{GS} = V_{DS}$$

$$I_{DS} \approx \beta_N(V_{DS}-V_{THN})^2$$



- Some elementary analog structures

Current mirror (based on NMOSFET or PMOSFET)

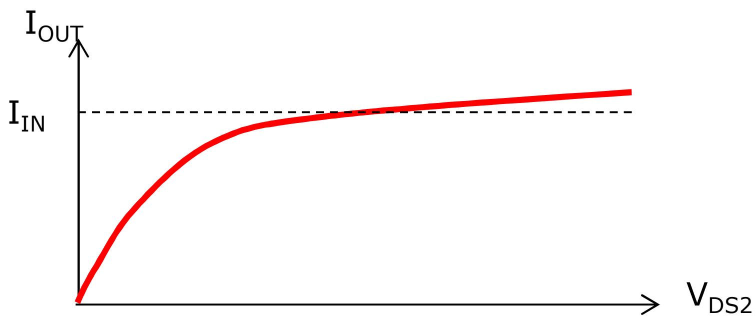



M1 and M2 have same characteristics, except dimensions W and L which can be different

$$\frac{W_2}{L_2} = K \frac{W_1}{L_1}$$

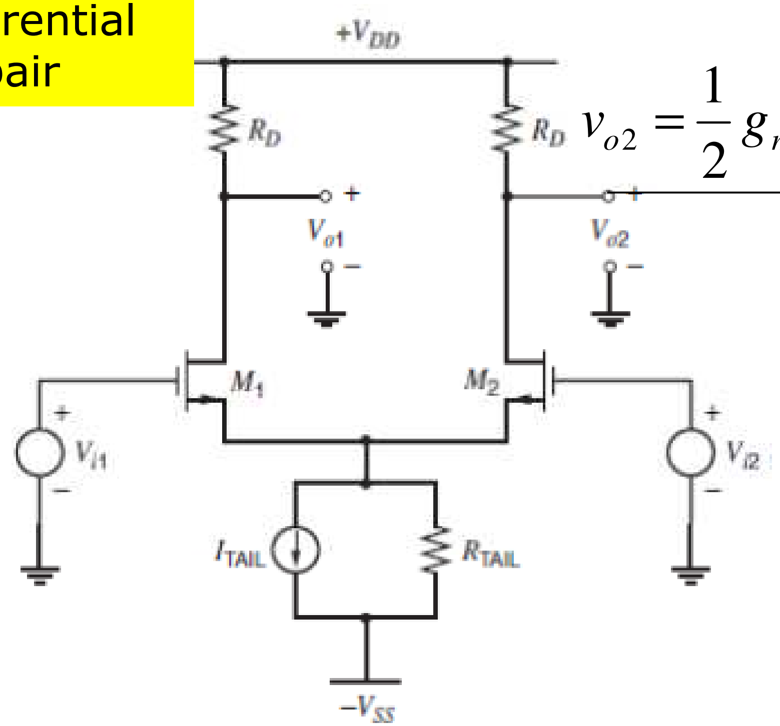
If M2 is in saturation and if its output conductance is null:

$$I_{OUT} = K \times I_{IN}$$



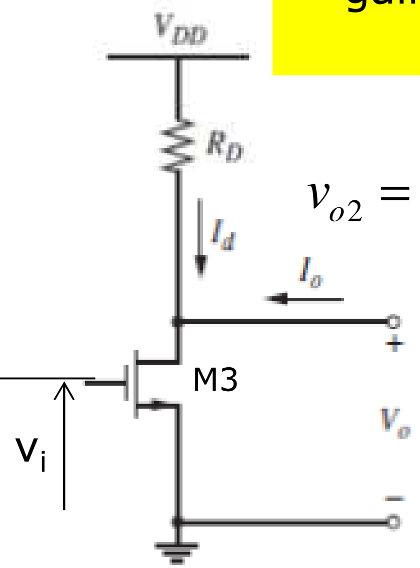
- Refer to book Gray, Hurst, Lewis, Meyer, « Analysis and Design of Analog Integrated Circuits », chapitres 6, 7, 8
- Principle of two-stage diff. Amplifier with single-ended output:

Differential pair




$$v_{o2} = \frac{1}{2} g_{m1} R_D v_{diff}$$

Output stage with gain (common-source)

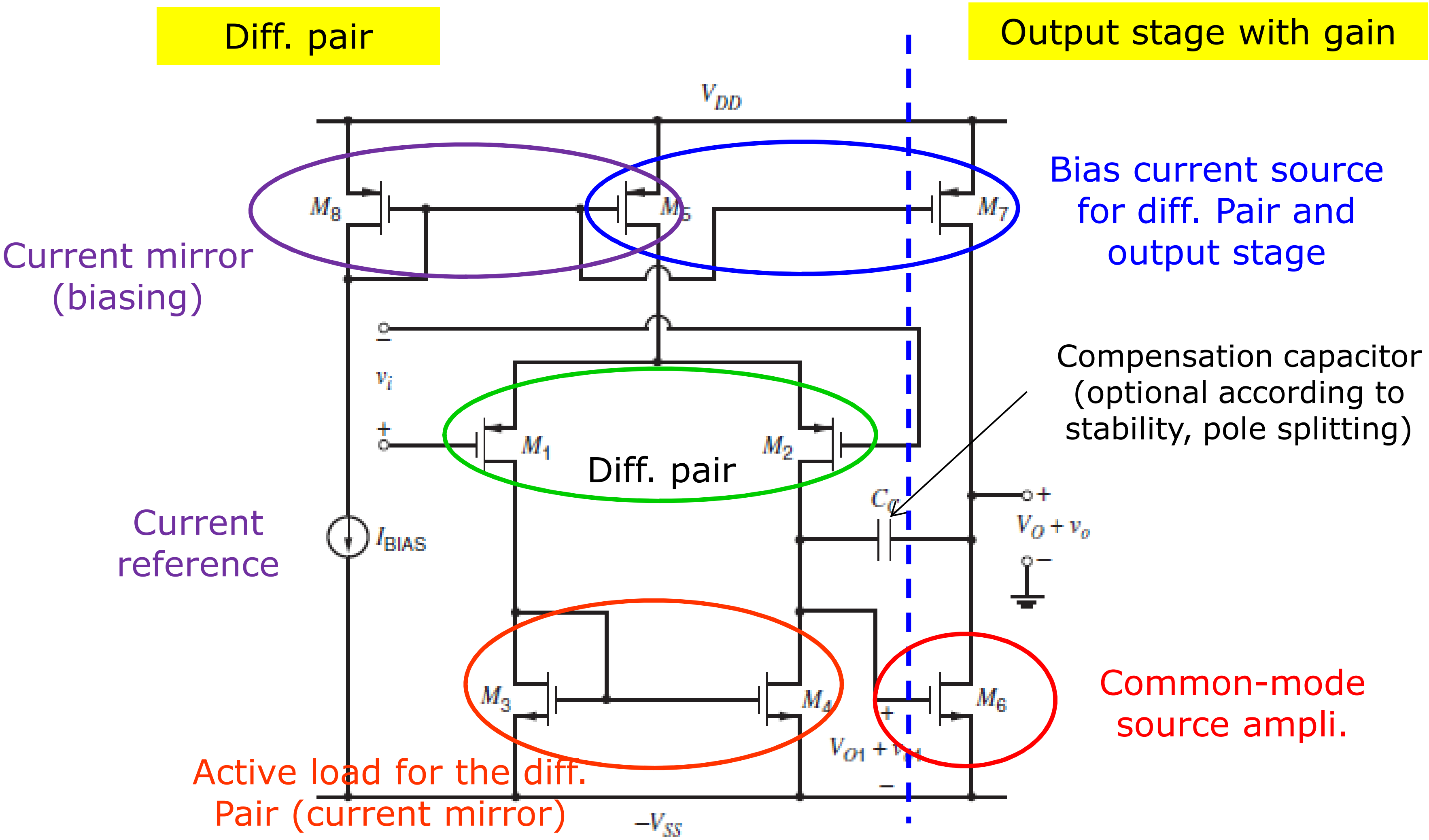



$$v_{o2} = -g_{m3}\left(r_0 // R_D\right) v_i$$

M1 and M2 are identical and in saturation, transconductance $g_{m1}$.

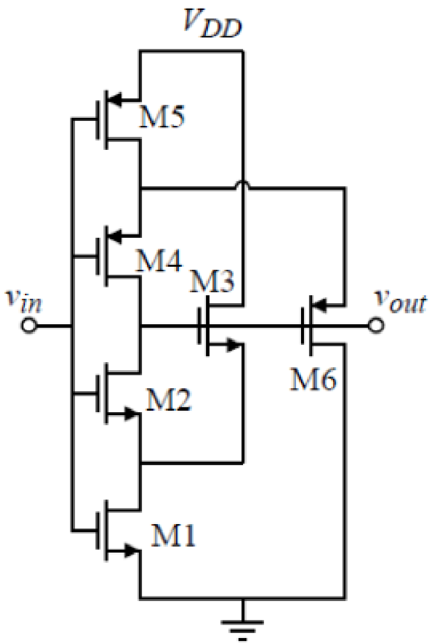
M3 saturated, transconductance $g_{m3}$, output resistance $r_0$

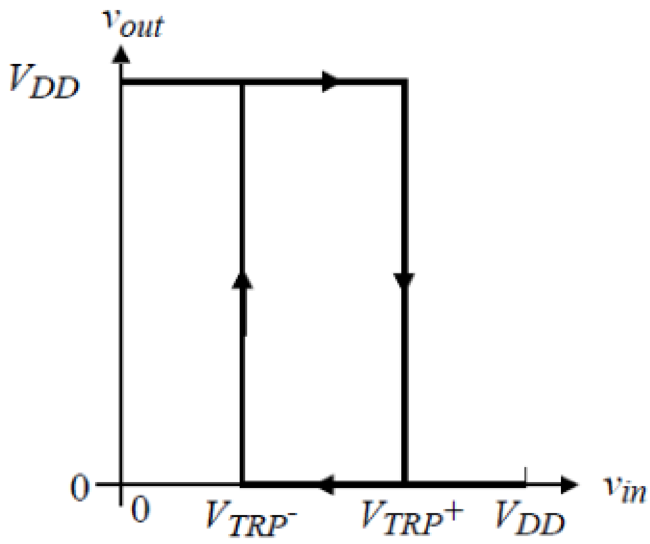
- Miller OTA amplifier (with PMOSFET diff. pair):



- Main characteristics to control:
  - Tatic gain
  - Output voltage range (rail-to-rail ideally)
  - Input/output offset
  - Common-mode rejection
  - Bandwidth, gain-bandwidth product
  - Open-loop transfer function, poles, stability (phase margin)
  - Slew rate
  - Power supply rejection ratio (PSRR)
  - Power consumption

- OPA based comparator (slew rate, offset issues…)
- <u>Schmitt trigger (digital structure):</u>



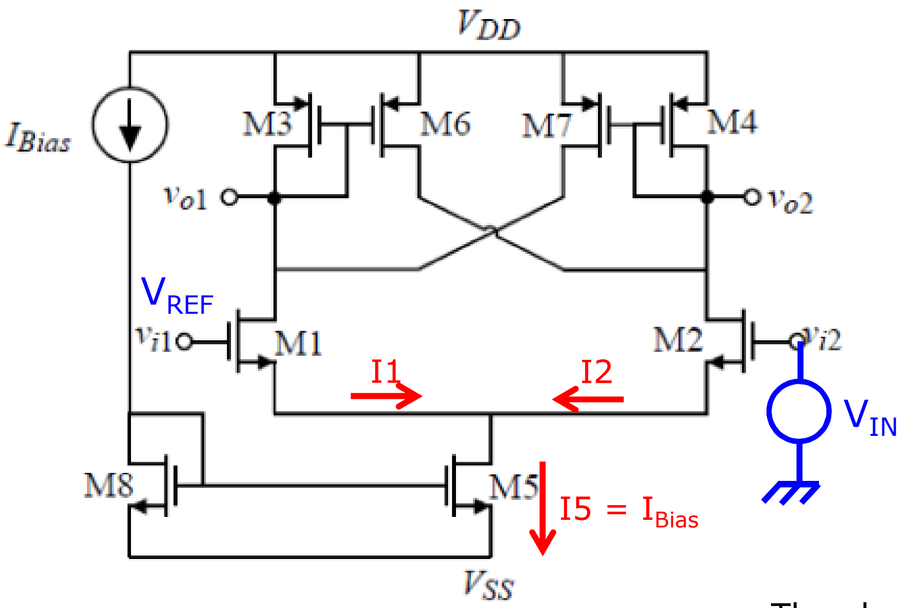



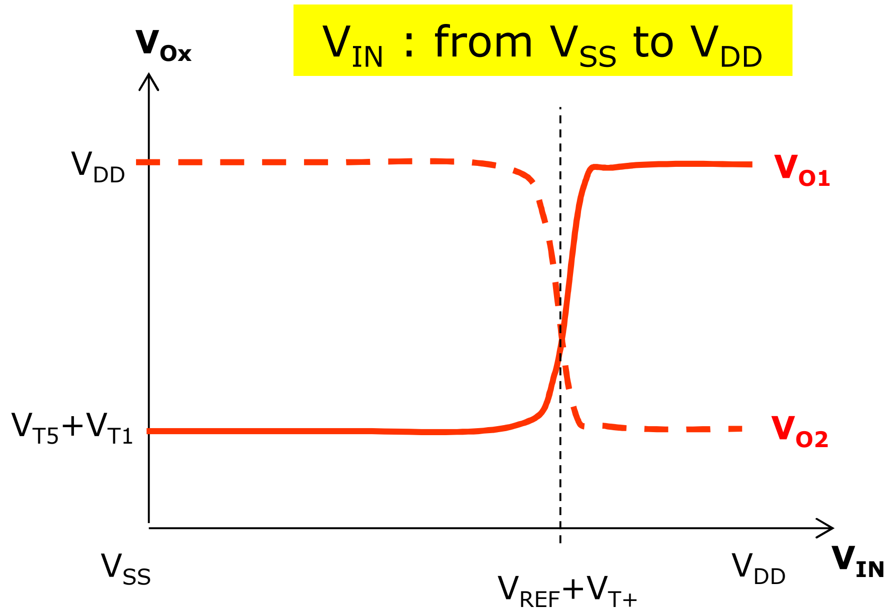

$$V_{TRP^-} = \frac{\sqrt{\beta_5/\beta_6}\,(V_{DD} - V_{TP5})}{1 + \sqrt{\beta_5/\beta_6}}$$

$$V_{TRP^+} = \frac{V_{TN1} + \sqrt{\beta_3/\beta_1}\,V_{DD}}{1 + \sqrt{\beta_3/\beta_1}}$$

With :
- ✓ $V_{Txx}$ = Threshold voltage($V_{TN2} = V_{TN3}$, $V_{TP4} = V_{TP6}$)
- ✓ $\beta x = ½\mu_x C_{ox} W/L$ = transconductance

- Internal hysteresis comparator




Conditions :

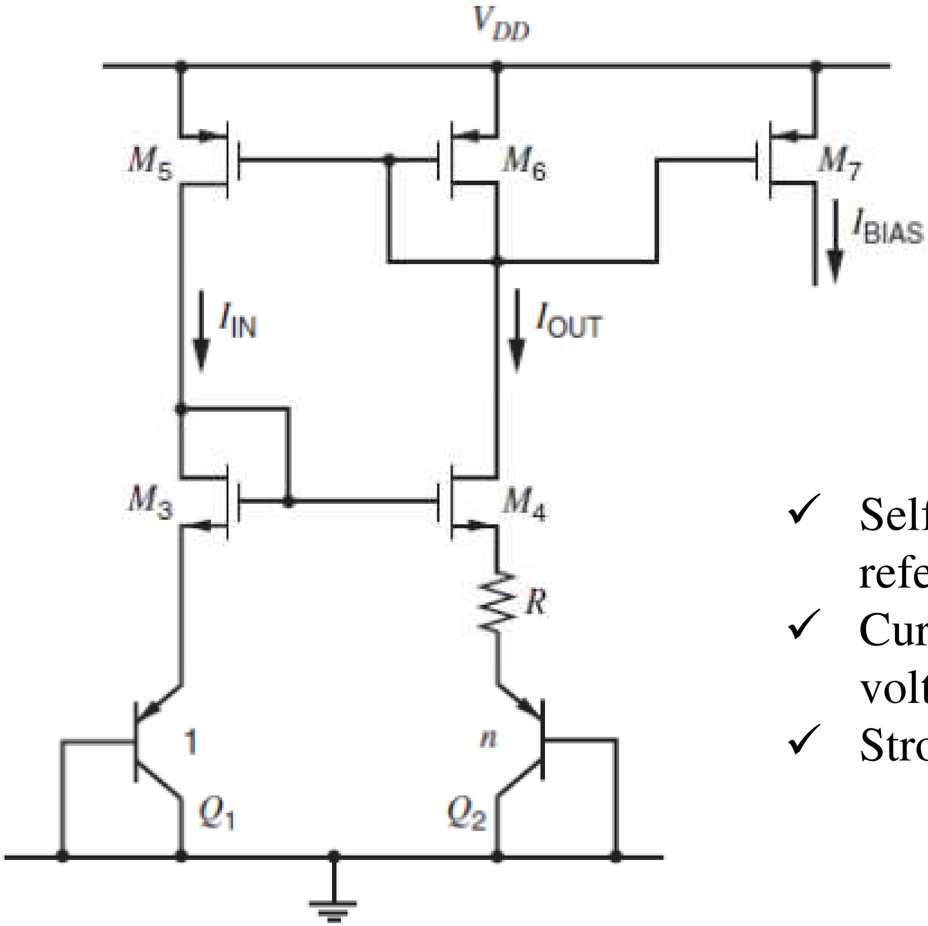
- ✓ M1 = M2
- ✓ M3 = M4
- ✓ M6 = M7
- ✓ $I5 = I_{Bias}$ = constant
- ✓ B1= M1 transconductance
- ✓ $$\frac{W_6/L_6}{W_3/L_3} = \frac{W_7/L_7}{W_4/L_4} = K$$

Threshold and hysteresis width:

$$V_{T+} = \sqrt{\frac{i_5}{\beta_1}}\,\frac{\sqrt{K}-1}{\sqrt{1+K}} \qquad V_{T-} = \sqrt{\frac{i_5}{\beta_1}}\,\frac{1-\sqrt{K}}{\sqrt{1+K}}$$

$$V_{T+} - V_{T-} = 2\sqrt{\frac{i_5}{\beta_1}}\,\frac{\sqrt{K}-1}{\sqrt{1+K}}$$

- Example: current reference




If M3 = M4 et M5 = M6 and in saturation :

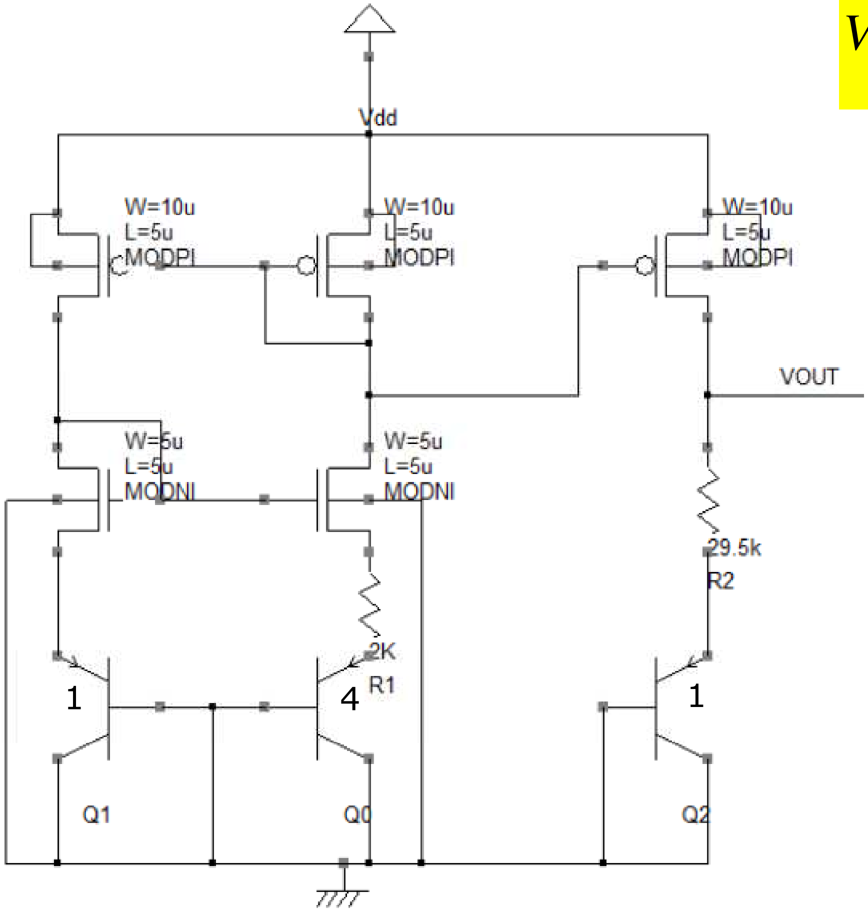
✓ $I_{IN} = I_{OUT}$

✓ $$I_{OUT} = \frac{kT}{q}\frac{\ln(n)}{R}$$

✓ If M7 = M6, $I_{BIAS} = I_{OUT}$

- ✓ Self-biased structure (no external current reference is required)
- ✓ Current weakly dependent on power supply voltage
- ✓ Strong dependence to temperature

- Example: bandgap voltage reference
- Reuse the previous current reference and adding of a temperature compensation strategy



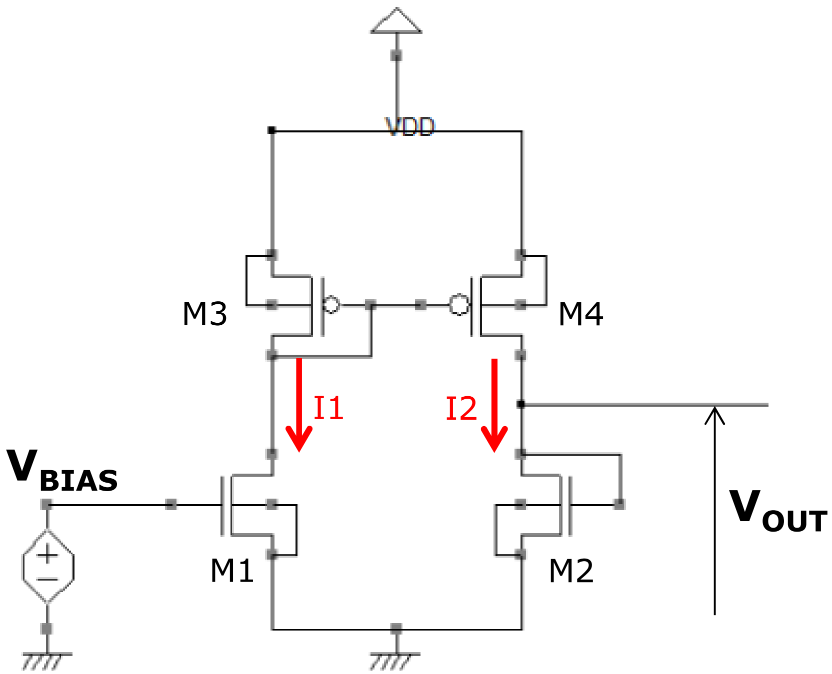

$$V_{OUT} = V_{EB2} + R_2 I_{OUT} = V_{EB2} + R_2 \frac{kT}{q} \frac{\ln(n)}{R}$$

✓Proportional To Absolute Temperature (PTAT) = voltage drop across R2 ($dV_{R2}/dT \approx +1.8$ mV/° c)

✓Complementary To Absolute Temperature (CTAT) = PNP-based diode ($dV_{EB}/dT \approx -2$ mV/° c)

VBE multiplier

- Fully CMOS temperature sensor: based on temperature depenceof $V_{TH}$




$$V_{TH} \approx V_{TH0} + \alpha(T - T_0), \alpha = -0.5..-2mV/°c$$

✓M1, M2, M3, M4 in saturation
✓If M3 = M4 → $I_1 = I_2$ (current mirror)
✓$V_{TH1} = V_{TH2}$

✓M2 is mounted as a diode:

$$V_{OUT} = V_{GS2} = \sqrt{\frac{I_2}{\beta_2}} + V_{TH2}$$

✓M1 controlled by Vbias → set the ibas current :

$$I_1 = \beta_1 (V_{BIAS} - V_{TH1})^2$$

$$V_{OUT} = \sqrt{\frac{\beta_1}{\beta_2}} V_{BIAS} + V_{TH}\left(1 - \sqrt{\frac{\beta_1}{\beta_2}}\right) \Rightarrow V_{TH} = \frac{V_{OUT} - \sqrt{\frac{\beta_1}{\beta_2}} V_{BIAS}}{1 - \sqrt{\frac{\beta_1}{\beta_2}}}$$